CS501- Advanced Computer Architecture
Final term Spring 2012

1. Define PROM? (2 Marks)

Answer:- (Page 356)

The PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into only once. For PROM, the writing process is performed electrically in the field. PROMs provide flexibility and convenience.

2. How we refer the register to the RTL? Give an example? (2 Marks)

Answer:- (Page 66)

Specifying Registers

The format used to specify registers is
Register Name<register bits>
For example, IR<31..0> means bits numbered 31 to 0 of a 32-bit register named "IR" (Instruction Register).

3. What is the use of modem? (2 Marks)

Answer:- (Page 391)

To interconnect different computers by using twisted pair copper wire, an interface is used which is called modem. Modem stands for modulation/demodulation. Modems are very useful to utilize the telephone network (i.e. 4 KHz bandwidth) for data and voice transmission.

4. What is the advantage of RAID level 0? (2 Marks)

Answer:- (Page 330)

• The user and system data are distributed across all the disks in the array.
• Notable advantage over the use of a single large disk.

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6. Encode the register into binary? R0 TO R7 (3 Marks)

Answer:- (Page 51)

Encoding of the General Purpose Registers.

R0	00000
R1	00001
R2	00010
R3	00011
R4	00100
R5	00101
R6	00110
R7	00111

7. What is the difference multimode fiber and mono fiber which are used as a physical medium of the network? (3 Marks)

Answer:- (Page 391)

Multimode fiber

This fiber has large diameter. When light is injected, it disperses, so the effective data rate decreases. Multimode fiber is used as a physical medium of the network

Mono mode Fiber

Its diameter is very small. So dispersion is small and data rate is very high.

8. What is meant by cycle stealing in the DMA? (3 Marks)

Answer:- (Page 320)

The DMA module takes control of the bus to transfer data to and from memory by forcing the CPU to temporarily suspend its operation. This approach is called Cycle Stealing because in this approach DMA steals a bus cycle.

10. Write the radix conversion algorithm to convert 392_{10} to the base 16? (5 Marks)

Answer:- (Page 335)

According to the above algorithm

390/16 =24(rem=6), x0=6

24/16= 1(rem=8), x1=8, x2=1

Thus 390_{10}

$=186_{16}$

11. What is the difference between internal segmentation and external segmentation relevant to the computer storage? (5 Marks)

Answer:-

In fixed partitioning the pages are of fixed size and some space is wasted in the last page. For example if we have page size equal to 2 K and the program size is of 9 K than we have to use 5 pages each of size 2 k. In this case 4 pages fully consumed but the last page has 1 k free memory and it can not be utilized, so this type of fragmentation is called internal fragmentation. It is basically the wastage of space of within the partition.

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In variable partitioning the page size is not fixed. In this type of partitioning the page size is variable. So pages are allocated accordingly. If say program A is of size 5 k than 5 k page size is reserved and say another program B comes in having size 3 k so now page size of 3 k is reserved. Now if A program exits and the new program C having size 4 k comes in, it will replace the 5 k partition of program A but the space of 1 K is wasted between program C and program B. This wastage of space is called external fragmentation. It is basically the wastage of space between the partitions.

12. Write the SRC assembly program for the following expression? (5 Marks)
Z= 16(a+b)-32(c-58)
Answer:- (According to Page 57)

```
ld R1, c     ; c is a label used for a memory location
subi R3, R1, 58     ; R3 contains (c-58)
shl R7, R3, 5    ; R7 contains 32(c-58)
ld R4, a
ld R5, b
add R6, R4, R5    ; R6 contains (a+b)
shl R8, R6, 4    ; R8 contains 16(a+b)
sub R9, R7, R8    ; the result is in R9
st R9, z    ; store the result in memory location z
```

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Q1-Write two lines on connection oriented communication? 2
Answer:- (Page 394)
In this method, same path is always taken for the transfer of messages.
It reserves the bandwidth until the transfer is complete. So no other server could use that path until it becomes free.

Q2-What is the advantage of direct cache memory? 2
Answer:- (Page 361)
Advantage is Simplicity.

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Q3-Write the drawbacks of DMA? 2

Answer:- (Page 315)

The disadvantage however, would be that an additional DMA controller would be required, that could make the system a bit more complex and expensive. Generally, the DMA requests have priority over all other bus activities including interrupts. No interrupts may be recognized during a DMA cycle.

Q4-What is the difference between selection channel and multiple channels? 3

Answer:- (Page 320)

Selector Channel

It is the DMA controller that can do block transfers for several devices but only one at a time.

Multiplexer Channel

It is the DMA controller that can do block transfers for several devices at once.

Q5-What is the advantage of linker in assembly language program? 3

Answer:- (Page 26)

When developing large programs, different people working at the same time can develop separate modules of functionality. These modules can then be 'linked' to form a single module that can be loaded and executed. The modularity of programs, that the linking step in assembly language makes possible, provides the same convenience as it does in higher-level languages; namely abstraction and separation of concerns. Once the functionality of a module has been verified for correctness, it can be re-used in any number of other modules. The programmer can focus on other parts of the program. This is the so-called "modular" approach, or the "top-down" approach.

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What do you know about PROM? Explain.(2 marks)

Answer:- Rep

What do you understand by the assembler of the assembly language? (2 marks)

Answer:- (Page 26)

Programs written in assembly language require translation to the machine language, and an assembler performs this translation. This conversion process is termed as the assembly process.

خدا کے سوا کسی سے امید مت رکھو

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Consider a LAN using bus topology if we replace the bus with a switch, what change occurs in such a configuration. (2 marks)

Answer:- (Page 385)

If we replace the bus with a switch, the speed of the data transfer will be improved to a great extent.

Name the two classes of instruction set architecture. (2 marks)

Answer:- (Page 32)

- Accumulator based machines
- Stack based machines

Find the average relational latency if the disk octet 15000rpm. (3 marks)

Answer:- (Page 324)

The average latency to the desired data is halfway round the disk so
Average rotational latency = (1 / (RPM / 60)) * 0.5 * 1000
= 30000 / RPM = 30000 / 15000
=2ms

How shift instructions are useful? When do we use them? (3 marks)

Answer:- (Page 18) click here for detail

Using shift instructions (shiftl, asr, etc.) is faster that **mul** and **div,** if the multiplier or divisor is a power of 2. Shift and logical instructions are used to implement logical expressions and bitwise logical operators in high level languages. Shift instructions for arithmetic operations are more efficient than the corresponding arithmetic instruction.

How the exception may be generated? Difference between external and internal exception.

Answer:- (Page 197)

Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.
External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Conceder the following point number

-6×10^{-3}

Find out the sign, significant and exponent from the above example. (3 marks)

Answer:- (Page 347)

Sign = -1
Significand= 6
Exponent= -3
Base = 10= fixed for given type of representation

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Does DMA affect the relationship between the memory system and the CPU? Explain (5 marks)

Answer:- (Page 321)

DMA and memory system

DMA disturbs the relationship between the memory system and CPU.

Direct memory access and the memory system

Without DMA, all memory accesses are handled by the CPU, using address translation and cache mechanism. When DMA is implemented into an I/O system memory accesses can be made without intervening the CPU for address translation and cache access. The problems created by the DMA in virtual memory and cache systems can be solved using hardware and software techniques.

Suppose the I/O system with a single disk get an average of 200 I/O request/second assume that the average time for a disk to service and I/O request is 4ms. What is the utilization of I/O system? (5marks)

Answer:- (Page 382)

Time for an I/O request = 4ms

=0.004sec

Server utilization = 200 x 0.004

= 0.8

Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines

a) How many sets are there in the cache?

b) How many bits of address are required to select a set in cache?

Answer:-

(a)

256 × 1024 ÷ 32 = 8192 lines of data

8192 / 4 = 2048 sets in the cache

A 256KB cache with 32 byte lines contains 8192 lines of data. In a 4-way set associative cache, each set contains 4 lines, so there are 2048 sets in the cache.

(b)

Log_2 (2048) =11. Hence 11 bits of the address are required to select the set.

زندگی میں کامیابی کا یہی راز ہے کہ پریشانیوں سے پریشان مت بنو

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1. The following table shows a partial summary of the ISA for the SRC. Write an assembly language program using the SRC assembly language to evaluate the expression: (5 marks)
Z= (7 + 16a) – (8b – c)
Answer:-
Answer:- (According to Page 57)

```
ld R1, c     ; c is a label used for a memory location
ld R2,b
shl R3,R2,3
sub R4, R3, R1
ld R5, a
shl R5,4
addi R6,R5,7
sub R7, R6, R4
st R7, z     ; store the result in memory location z
```

Find the bandwidth of a memory system that has a latency of 30ns, a pre charge time of 10ns and transfers 3 bytes of data per access. (5 marks)
Answer:-
Time between two memory reference
= latency + pre charge time
=30ns+10ns
= 40ns

Throughput = 1/40ns
$=2.5 \times 10^7$ operation/sec

Bandwidth= $3*2.5 \times 10^7$
$= 7.5 \times 10^7$ byets/sec

2. Explain the Direct Mapping cache strategy. (5 marks)
Answer:- (Page 360)
In this technique, a particular block of data from main memory can be placed in only one location into the cache memory. It relies on principle of locality.
Cache address is composed of two fields:
• Group field
• Word field
Valid bit specifies that the information in the selected block is valid.

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3. How many platters are required for a 40GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter? (5 marks)

Answer:- (Page 325)

The capacity of one platter
= 1024 x 2048 x 4096
= 8GB
For a 40GB hard disk, we need 40/8
= 5 such platters.

1. What do you understand by RAID 2? (3 marks)

Answer:- (Page 331)

In RAID 2, error-correcting code is calculated across corresponding bits on each data disk.

2. Give an example for the logic design level, circuit level and mask level abstractions of digital design. (3 marks)

Answer:- (Page 22)

Logic Design Level
The logic design level is also called the gate level. The basic elements at this level are gates and flip-flops. The behavior is less visible, while the hardware structure predominates.
The above level relates to "logic design".

Circuit Level
The key elements at this level are resistors, transistors, capacitors, diodes etc.

Mask Level
The lowest level is mask level dealing with the silicon structures and their layout that implement the system as an integrated circuit.
The above two levels relate to "circuit design".

3. Differentiate between Spatial Locality And Temporal Locality. (3 marks)

Answer:- (Page)

Spatial Locality
This would mean that in a part of a program, if we have a particular address being accessed then it is highly probable that the data available at the next address would be highly accessed.

Temporal Correlation
In this case, we say that at a particular time, if we have utilized a particular part of the memory then we might access the adjacent parts very soon.

4. Suppose an I/O system with a single disk gets (on average) 200 I/O requests/second. Assume that average time for a disk to service an I/O request is 4ms. (3 marks)

Answer:- Rep

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What is the utilization of the I/O system? (3 marks)

Answer:- (Page 381)

Server Utilization = Arrival Rate x $Time_q$

Server utilization is also called traffic intensity and its value must be between 0 and 1.

Server utilization depends upon two parameters:

1. Arrival Rate
2. Average time required to serve each task

So, we can say that it depends on the I/O bandwidth and arrival rate of calls into the system.

1. Which term do we use to describe a "storage systems" resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques? (2 marks)

Answer:- click here for detail

RAID is the term used to describe a storage systems' resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques.

2. Differentiate between CPU register and Cache Memory. (2 marks)

Answer:- (Page 33)

In general purpose register machines, a number of registers are available within the CPU. These registers do not have dedicated functions, and can be employed for a variety of purposes. CPU registers are faster than cache memory.

Cache memory is random access memory (RAM) that a computer microprocessor can access more quickly than it can access regular RAM.

3. Write one advantage and one disadvantage of cache design. (2 marks)

Answer:- (Page 361)

Advantage:

Simplicity

Disadvantage:

Only a single block from a given group is present in cache at any time. Direct map Cache imposes a considerable amount of rigidity on cache organization.

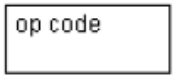
4. What is the format of a 0-address instruction set? (2 marks)

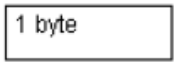
Answer:- (Page 36)

0-address instruction

- The code size is 1 byte
- Number of bytes accessed from memory is 10

(1 byte for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 10 bytes)





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How many drives do you need a minimum to form RAID 0? (2 marks)
0
Only 1
Minimum 2
Maximum 2
Answer:- click here for detail
Minimum 2
To establish a RAID 0 volume, a minimum of at least 2 hard disk drives are required. Unlike RAID 1, the number of drives used in the array can be an odd or even number.

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What function is performed by the reset operation of a processor? What are the two types of reset operations?
Answer:- (Page 194-195)
The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Hard Reset
The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes the PC and the general registers.

Soft Reset
The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.
The reset signal in SRC is assumed to be external and asynchronous.

Q2 What do you know about Hard disk.
Answer:- (Page 323)
Peripheral devices connect the outside world with the central processing unit through the I/O modules. One important feature of these peripheral devices is the variable data rate. Peripheral devices are important because of the function they perform.
A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

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Q 3 :- Convert $(0.23)_{10}$ to the base 2 address 2Marks

Answer:- (page 336)

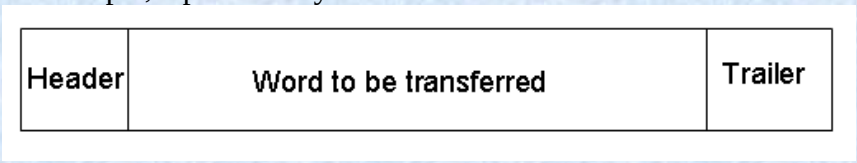
0.23*2=0.46, $f_{-1}=0$
0.46*2=0.92, $f_{-2}=0$
0.92*2=1.84, $f_{-3}=1$
0.84*2=1.68, $f_{-4}=1$
0.68*2=1.36, $f_{-5}=1$, …
Thus $0.24_{10} = (0.00111)_2$

Question no 4

What is meant by Packet switching

Answer:- (Page 387)

A block (an appropriate number of bits) of data is called a packet. Transfer of data in the form packets through different paths in a network is called packet switching. Additional bits are usually associated with each packet. These bits contain information about the packet. These additional bits are of two types: header and trailer. As an example, a packet may have the form shown below:



If we use a 1- bit header, we may have the following protocol:
Header = 0, it means it is a request
Header = 0, Reply
By reading these header bits, a machine becomes able to receive data or supply data. To transfer data by using packets through hardware is very difficult. So all the transfer is done by using software. By using more number of bits, in a header, we can send more messages. For example if n bits are used as header then 2^n is the number of messages that can be transmitted over a network by using a single header.
For a 2 bit header: we may have 4 types of messages:
00= Request
01= Reply
10= Acknowledge request
11= Acknowledge reply

Question no 6

Classification of fiber optics mode multimode and mono mode?

Answer:- Rep

Question no 7

Consider a 64KB direct-mapped cache with a line length of 32 bytes. (5 marks)
a. Determine the number of bits in the address that refer to the byte within a cache line.
b. Determine the number of bits in the address required to select the cache line

جھوٹ انسان اور ایمان دونوں کا دشمن ہے

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Answer:- (Page 375)
Address breakdown
n=$\log_2$ of number of bytes in line
m=$\log_2$ of number of lines in cache
a. For the given cache, the number of bits in the address to determine the byte within the line= n = $\log_2 32 = 5$

b. There are 64K/32= 2048 lines in the given cache. The number of bits required to select the required line = m =$\log_2 2048 = 11$
Hence n=5 and m=11

Question no 8
If a DRAM has 512 rows and its fresh time is 9ms .What shoul be the frequency of row refresh operation on the average?
Answer:- (Page 371)
Refresh time =9ms
Number of rows =512
Therefore we have to do 512 row refresh operations in a 9 ms interval, in other words one row refresh operation every ($9*10^{-3}$)/512=$1.76 * 10^{-5}$ second

Question
Structural RTL for not instruction not ra ,rb
Answer:- (Page 160)

Step	RTL
T0-T2	Instruction fetch
T3	C ← !(R[rb]);
T4	R[ra] ← C;

Question
why we use matrix in decoder
Answer:- (Page 352)
A typical one level decoder has n inputs and 2_n output, using one level of gates, each with a fan-in of n. Two level decoders are limited in size because of high gate fan-in. In order to reduce the gate fan-in to a value of 8 or 6, tree and matrix decoders are utilized.

عقل مند کہتا ہے میں کچھ نہیں جانتا جبکہ بے وقوف کہتا ہے کہ میں سب کچھ جانتا ہوں

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41.**What are the functions of memory cell? 2 marks**

Answer:- (Page 351)

A memory cell provides four functions: Select, DataIn, DataOut, and Read/Write. DataIn means input and DataOut means output. The select signal would be enabled to get an operation of Read/Write from this cell.

What is Packet Switching? 2 marks

Answer:- Rep

43. **How we can specify registers in RTL? Give an example? 2 marks**

Answer:- (Page 66)

Specifying Registers

The format used to specify registers is
Register Name<register bits>
For example, IR<31..0> means bits numbered 31 to 0 of a 32-bit register named "IR" (Instruction Register).

44. **What is seek time of hard disk? 3 marks**

Answer:- (Page 323)

When it is required to read data from a particular location of the disk, the head moves towards the selected track and this process is called seek. The disk is constantly rotating at a fixed speed. After a short time, the selected sector moved under the head. This interval is called the rotational delay. On the average, the data may be available after half a revolution. Therefore, the rotational latency is half revolution.
The time required to seek a particular track is defined by the manufacturer. Maximum, minimum and average seek times are specified. Seek time depends upon the present position of the head and the position of the required sector. For the sake of calculations, we will use the average value of the seek time.

45. **Differences between RAID2 and RAID 3? 3 marks**

Answer:- (Page 331)

• In RAID 2, error-correcting code is calculated across corresponding bits on each data disk.
• RAID 3 requires only a single redundant disk.
• Instead of an error-correcting code, a simple parity bit is computed for the set of individual bits in RAID 3

46. **What are three main functions of control Unit? 3marks**

Answer:- click here for detail

It directs the entire computer system to carry out stored program instructions.
It must communicate with both the arithmetic logic unit (ALU) and the main memory.
It instructs the ALU on arithmetic operations to be performed.

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47. Difference between Spatial Locality and Temporal Correlation? 3 marks
Answer:- Rep

48. **How shift instructions are useful? When we use them? 3 marks**
Answer:- Rep

49.**Assume there is an accumulator based machine in which there are eight general purpose registers of the CPU. Each register is 16-bits in length. Also there are two additional 16-bit system registers which are the program counter (PC) and the instruction register (IR). The size of the memory word is 16-bit. Using yours knowledge of processor design process, answer the following question.**

Which name convention will you use to name each of these eight general purpose registers?
What is the available memory space size knowing that memory word is 16 bits? 5 marks

Answer:- (Page 112)
a)As the length of register is 16-bit so we use Little-endian name convention
b)memory word is 16-bit so the available memory space size is 2^{16} bytes

50. **Find the bandwidth of a memory system that has a latency of 30ns, a pre charge time of 10ns and transfers 3 bytes of data per access. 5 marks**
Answer:- Rep

51.**Using radix conversion algorithm converts 392_{10} to base 16… 5 marks**
Answer:-

52. **Differentiate between internal and external fragmentation 5**
Answer:- Rep

خود کو تمھیں سے بڑھ کر کوئی اچھا مشورہ نہیں دے سکتا

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How can overflow occur in floating point? (2 Marks)
Answer:- (Page 348)
Overflow occurs when the exponent is too large and can not be represented in the exponent field.

What is Packet Switching? (2 Marks)
Answer:- Rep

Difference between Eagle and modified Eagle (2 Marks)
Answer:- (Page 120)
The modified EAGLE is an improved version of the processor EAGLE. As we have already discussed, there were several limitations in EAGLE, and these have been remedied in the modified EAGLE processor.

Why we represent sometime some numbers in sign magnitude form.
Answer:- (Page 336)
• This is the simplest form for representing a signed number
• A symbol representing the sign of the number is appended to the left of the Number
• This representation complicates the arithmetic operations

(3 Marks Questions)
What is 4-address instruction set and when it use?
Answer:- (Page 36)

Discussion4-address instruction

- The code size is 13 bytes (1+3+3+3+3 = 13 bytes)
- Number of bytes accessed from memory is 22 (13 bytes for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 22 bytes)

op code	destination	source 1	source 2	next address
1 byte	3 bytes	3 bytes	3 bytes	3 bytes

Note that there is no need for an additional memory access for the operand corresponding to the next instruction, as it has already been brought into the CPU during instruction fetch.

جو شخص ناکامیوں سے ڈر کر بھاگتا ہے کامیابی اُس سے ڈر کر بھاگتی ہے

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Difference between virtual address and physical address
Answer:- (Page 321)
Virtual Address:
Virtual address is generated be the logical by the memory management unit for translation.
Physical Address:
Physical address is the address in the memory.

Why Transaction Lockaside Buffer is used? How it is implemented inside CPU?
Answer:- (Page 368)
Identifying a particular page in the virtual memory requires page tables (might be very large) resulting in large memory space to implement these page tables. To speed up the process of virtual address translation, translation Lookaside buffer (TLB) is implemented as a small cache inside the CPU, which stores the most recent page table entry reference made in the MMU. It contents include
• A mapping from virtual to physical address
• Status bits i.e. valid bit, dirty bit, protection bit
It may be implemented using a fully associative organization

What is sender overhead and receiver overhead in computer networks?
Answer:- (Page 388)
Sender overhead
It is the time for the processor to inject message in to the network.
Receiver overhead
It is the time for the processor to pull the message from the network.

5 Marks Questions

Find the average access time of a level of memory hierarchy if the hit rate is 80%. The memory access takes 12ns on a hit and 100ns on a miss.
Answer:- (Page 372)

Hit rate =80%
Miss rate=20%
T_{hit}=12 ns
T_{miss}=100ns
Average T_{access}=(hit rate*T_{hit})+(miss rate*T_{miss})
=(0.8*12ns)+(0.2*100ns)
= 29.6ns

جو لوگوں کے سامنے فخر کرتا ہے وہ لوگوں کی نظروں سے گر جاتا ہے

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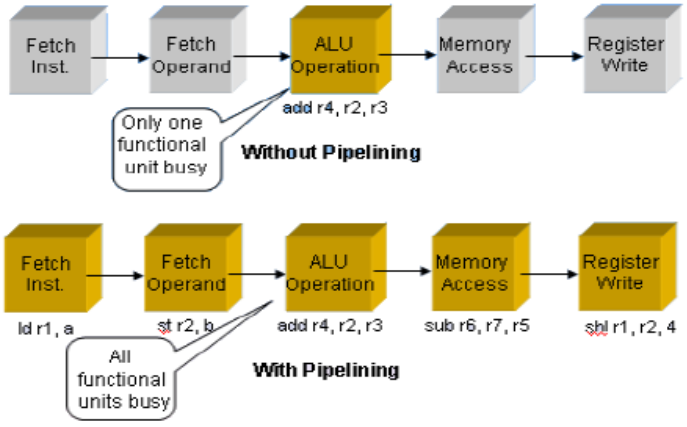
What is difference of instruction in machine with and without Pipeline?
Answer:- (Page 202)

Executing machine instructions with and without pipelining

We start by assuming that a given processor can be split in to five different stages as shown in the diagram below, and as explained later in this section. Each stage receives its input from the previous stage and provides its result to the next stage. It can be easily seen from the diagram that in case of a non-pipelined machine there is a single instruction **add r4, r2, r3** being processed at a given time, while in a pipelined machine, five different instructions are being processed simultaneously. An implied assumption in this case is that at the end of each stage, we have some sort of a storage place (like temporary registers) to hold the results of the present stage till they are used by the next stage.



Convert $(0.23)_{10}$ to the base 2 address.
Answer:- Rep

Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines
a) How many sets are there in the cache?
b) How many bits of address are required to select a set in cache?
Answer:- Rep

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Q 1: Consider 64KB direct mapped cache, line length 32 bytes, and find the number of bits in the address. 2
Answer:- Rep

عقل مند اپنے عیب خود دیکھتا ہے اور بیوقوفوں کے عیب دنیا دیکھتی ہے

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Q 2: Define virtual memory 2

Answer:- (Page 364)

Virtual memory acts as a cache between main memory and secondary memory. Data is fetched in advance from the secondary memory (hard disk) into the main memory so that data is already available in the main memory when needed. The benefit is that the large access delays in reading data from hard disk are avoided.

Q 3: What does the RTL expression M [1234] means 2

Answer:- click here for detail

The RTL expression [M(1234)] means the contents of memory whose location (i.e., address) is 1234. Or, sometimes expressed as 0x1234 to denote hex.

Q 4: What are the sectors of the hard disk? 2

Answer:- (Page 323)

A hard disk is the most frequently used peripheral device. It consists of a set of platters.
Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address.

Q 5: Why MIPS is not very accurate basis for comparison of different processes. Write formula of MIPS. 3

Answer:- (Page 45)

MIPS = IC/ (ET x 10_6)

This measure is not a very accurate basis for comparison of different processors. This is because of the architectural differences of the machines; some machines will require more instructions to perform the same job as compared to other machines. For example, RISC machines have simpler instructions, so the same job will require more instructions. This measure of performance was popular in the late 70s and early 80s when the VAX 11/780 was treated as a reference.

Q 6: Record the integer 485 according to the BOOTH procedure 3

Answer:- (Page 343)

Solution
Original number:
00111100101=256+128+64+32+4+1=485
Recoded Number:

$\bar{0}1\bar{0}0\bar{0}1\bar{0}1111$=+512-32+8-4+2-1=485

Q 7: Find out sign, significand and exponent of -7×10^{-4}. 3

Answer:-

Sign = -1
Significand= 7
Exponent= -4
Base = 10

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Q 8: Calculate Bandwidth, given Latency 30ns, per charge time is 10ns and 3 bytes of data per access. 5
Answer:- Rep

Q 9: Convert 0.23_{10} to base 2 5
Answer:- Rep

Q 10: Differentiate between internal and external fragmentation 5
Answer:- Rep

Q 11: Solve the instruction z = 5(a-b) +17(c+26) using
1 address instruction
0 address instruction.

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(2)
where TCP/IP Used??
Answer:- (Page 396)
Internet uses TCP/IP protocol. In the TCP/IP model, session and presentation layers are not present, so Store-Forward routing is used.

define PROM
Answer:- Rep

(3)
STAGes in pipelined SRC
Answer:- (Page 206)
The SRC uses a five-stage pipeline. Those five stages are given below:
1. Instruction Fetch
2. Instruction decode/operand fetch
3. ALU operation
4. Memory access
5. Register write

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diff bw serial and parallel transfer
Answer:- (Page 396)
Serial Transfer, or serial communication of data between the CPU and the I/O devices, refers to the situation when all the data bits in a "piece of information", (which is a byte or word mostly), are transferred one bit at a time, over a single pair of wires.

Parallel Transfer, or parallel communication of data between the CPU and the I/O devices, refers to the situation when all the bits of data (8 or 16 usually), are transferred over separate lines simultaneously, or in parallel.

configuration of 1x8 memory
Answer:- (Page 351)

1×8 Memory Cell Array (1D)
In this arrangement, each block is connected through a bi-directional data bus implemented with 2 tri-state buffers. $R/\overline{W}$ and Select signals are common to all these cells. This 1-dimentional memory array could not be very efficient, if we need to have a very large memory.

Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines
a) How many sets are there in the cache?
b) How many bits of address are required to select a set in cache?
Answer:- Rep

5)
difference bw connection oriented and connection less
Answer:- (Page 394)
Connection Oriented Communication
• In this method, same path is always taken for the transfer of messages.
• It reserves the bandwidth until the transfer is complete. So no other server could use that path until it becomes free.
• Telephone exchange and circuit switching is the example of connection oriented communication.
Connection less Communication
• Here message is divided into packets with each packet having destination address.
• Each packet can take different path and reach the destination from any route by looking at its address.
• Postal system and packet switching are examples of connection less communication.

بد صورت چہرہ بد صورت دماغ سے بہتر ہے

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compare 1D AND 2D

Answer:- (Page 351)

1×8 Memory Cell Array (1D)

In this arrangement, each block is connected through a bi-directional data bus implemented with 2 tri-state buffers. $R/\overline{W}$ and Select signals are common to all these cells. This 1-dimentional memory array could not be very efficient, if we need to have a very large memory.

4×8 Memory Cell Array (2D)

In this arrangement, 4×8 memory cell array is arranged in 2-dimensions. At the input, we have a 2×4 decoder. Two address bits at the input A0 and A1 would be decoded into 4 select lines. The decoder selects one of four rows of cells and then $R/\overline{W}$ signal specifies whether the row will be read or written.

write RTL for five instructions

movi R3,45

In R3,57

OUT R6 15

RET R3

ANDI R5 , R4. 5

Answer:- (Page 93)

movi R3,45

R[3] ← 56

In R3,57

R [3] ← IO [57]

OUT R6 15

IO [16] ← R [6]

RET R3

PC ← R [3]

ANDI R5 , R4. 5

R [5] ← R [4] & 5

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Differentiate b/w RISC n CISC according to their instruction size and hardware, software? 5 marks.
Answer:- **Click here for detail**

CISC	RISC
Emphasis on hardware	Emphasis on Software
Include multi-clock	Include Single-clock
complex instructions	Reducedinstructions only
memory to memory:	Registors to Register:
"LOAD" and "STORE"incorporated in instructions	"LOAD" and "STORE"are independent instructions
Small code sizes	Large code sizes
high cycles per second	Low cycles per second
Transistors used for storing	Spend more transistors on memory registors

RISC	CISC
Multiple register sets, often consisting of more than 256 registers	Single register set, typically 6 to 16 registers total
Three register operands allowed per instruction (e.g., `add R1, R2, R3`)	One or two register operands allowed per instruction (e.g., `add R1, R2`)
Parameter passing through efficient on-chip register windows	Parameter passing through inefficient off-chip memory
Single-cycle instructions (except for `load` and `store`)	Multiple-cycle instructions
Hardwired control	Microprogrammed control
Highly pipelined	Less pipelined
Simple instructions that are few in number	Many complex instructions
Fixed length instructions	Variable length instructions
Complexity in compiler	Complexity in microcode
Only load and store instructions can access memory	Many instructions can access memory
Few addressing modes	Many addressing modes

TABLE 9.1 The Characteristics of RISC Machines versus CISC Mach

بہترین تجربہ وہ ہے جس سے نصیحت حاصل ہو

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A hard disk with 5 platters has 1024 tracks per platter,512 sectors per track and 512 bytes/sector. What is the total capacity of the disk? 5 marks.

Answer:- (Page 324)

512 bytes x 512
sectors=0.2MB/track
0.2MB x 1024 tracks=0.2GB/platter
Therefore the hard disk has the total capacity of 5 x 0.2=1GB

What is the function of Control unit? 3 marks.

Answer:- Rep

What is the difference between control unit n data path? 2 mark

Answer:- (Page 150)

The data path design involves decisions like the placement and interconnection of various registers, the type of flip-flops to be used and the number and kind of the interconnection buses.
The control unit design is a rather tricky process as it involves timing and synchronization issues besides the usual combinational logic used in the data path design.

What is the working of DMA controller? 5 marks

Answer:- (Page 314)

A DMA controller could be a CPU in itself and it could control the total activity and synchronize the transfer of data". DMA could be considered as a technique of transferring data from I/O to memory and from memory to I/O without the intervention of the CPU. The CPU just sets up an I/O module or a memory subsystem, so that it passes control and the data could be passed on from I/O to memory or from memory to I/O or within the memory from one subsystem to another subsystem without interaction of the CPU. After this data transfer is complete, the control is passed from I/O back to the CPU.

Define 64K x 1 static RAM chip? 5 marks.

Answer:- (Page 352)

A 64k×1 Static RAM Chip

The cell array is indicated as 256 × 256. So, there would be 256 rows and 256 columns. A 64k × 1 cell array requires 16 address lines, a read/write line, $R/\overline{W}$, a chip select line, CS, and only a single data line. The lower order 8-address lines select one of the 256 rows using an 8-to-256 line row decoder. Thus the selected row contains 256 bits. The higher order 8-address lines select one of those 256 bits. The 256 bits in the row selected flow through a 256-to-1 line multiplexer on a read. On a memory write, the incoming bit flows through a 1-to-256 line demultiplexer that selects the correct column of the 256 possible columns.

خوبصورتی علم وادب سے ہوتی ہے لباس و حسن سے نہیں

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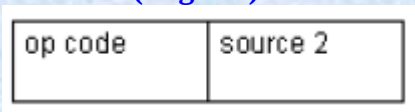
Format of the 1-Address instruction set-----2 Marks
Answer:- (Page 35)



What attributes should have a device to qualify in order to be master device ---- 2 Marks
Answer:- (Page 317)
A Master must have the capability to place addresses on the address bus and direct the bus activity during a bus cycle.

A network is suing the Bus topology if we replace the bus with switch what change will be take effects by this configuration…. 2 Marks
Answer:- Rep

What is ISA explain….. 2 marks
Answer:- (Page 28)
This set of instructions or operations and the resources together form the instruction set architecture (ISA). It is the ISA, which serves as an interface between the program and the functional units of a computer, i.e., through which, the computer's resources, are accessed and controlled.

Explain the relation ship between the Hard disk tracks, cylinders and sectors…3 marks
Answer:- (Page 323)
A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

Explain 1bit half adder function ……3 marks
Answer:- (Page 339)
It takes two
1-bit inputs x and y and as a result, we get a 1-bit sum and a 1-bit carry. This circuit is called a half adder because it does not take care of input carry. In order to take into account the effect of the input carry, a 1-bit full adder is used which is also shown in the figure. We can add two m-bit numbers by using a circuit which is made by cascading m 1-bit full adders.

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SRS assembly program for the following expiration..5 Marks
Z = 13(A+B)-32(c-58)
Answer:- (Page 57)

```
ld R1, c     ; c is a label used for a memory location
subi R3, R1, 58     ; R3 contains (c-58)
shl R7, R3, 5    ; R7 contains 32(c-58)
ld R4, A
ld R5, B
add R6, R4, R5    ; R6 contains (A+B)
```

Notice that the SRC does not have a multiply instruction. We will make use of the fact that multiplication with powers of 2 can be achieved by repeated shift left operations. But in the given example 13 is not directly is a power of 2. So you need to make it power of 2.
13(A+B) = 8(A+B) + 4 (A+B) + (A+B)
Suppose we place A+B in some register say R6.

```
Shl R7, R6, 3;            ;8 (A+B)
Shl R8, R6, 2;            ;4 (A+B)
Add R10, R8, R7;      ;8 (A+B) + 4 (A+B)
Add R11, R6, R10;    ;8 (A+B) + 4 (A+B) + (A+B)that is equal to 13((A+B))
sub R12, R7, R11
st R12, z    ; store the result in memory location z
```

Latency of the ram is 30ns , if the time charge is 10ns and data pre change is 3 byte then find the band width…5 Mrks
Answer:- Rep

Compare the 1 x 8 bit Memory (1D) and 4 x 8 Memory (2D) 5 marks
Answer:- Rep

تم اچھا کرو زمانہ تم کو برا سمجھے یہ اس سے بہتر ہے کہ تم برا کرو اور زمانہ تم کو اچھا سمجھے

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Consider a 64KB direct-mapped cache with a line length of 32 bytes. (5 marks)
a. Determine the number of bits in the address that refer to the byte within a cache line.
b. Determine the number of bits in the address required to select the cache line
Answer:- Rep

Comparisons of FALCON-A and SRC (5 marks)
Answer:- (Page 272)

Comparisons of the SRC and FALCON-A Examples

The FALCON-A and SRC programmed I/O examples discussed are similar with some differences. In the first example discussed for the SRC (i.e. Character output), the control signal responsible for data transfer by the CPU is the ready signal while for FALCON-A Busy (active low)signal is checked. In the second example for the SRC, the instruction set, address width and no. of lines on address is different. Although different techniques have been used to increase the efficiency of the programmed I/O, overheads due to polling can not be completely eliminated.

How many platters are required for a 40GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter (5)
Answer:- Rep

What is difference between hard disk, cylinder, sector (3 makrs)
Answer:- Rep

How to Virtual Memory work? Briefly define? (3 marks)
Answer:- Rep

Differences between RAID2 and RAID 3 (3 marks)
Answer:- Rep

What is Cache? How does it works? (3 marks)
Answer:- (Page 356)
Cache by definition is a place for safe storage and provides the fastest possible storage after the registers. The cache contains a copy of portions of the main memory. When the CPU attempts to read a word from memory, a check is made to determine if the word is in the cache. If so, the word is delivered to the CPU. If not, a block of the main memory, consisting of some fixed number of words, is read into the cache and then the word is delivered to the CPU.

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Cache Management (2 marks)
Answer:- (Page 339)
To manage the working of the cache, cache control unit is implemented in hardware, which performs all the logic operations on the cache. As data is exchanged in blocks between main memory and cache, four important cache functions need to be defined.

Block Placement Strategy
Block Identification
Block Replacement
Write Strategy

What is EPROM (3 marks)
Answer:- (Page 356)
Erasable Programmable Read-only Memory or EPROM chips have quartz windows and by applying ultraviolet light erase the data can be erased from the EPROM. Data can be restored in an EPROM after erasure. EPROMs are more expensive than PROMs and are generally used for prototyping or small-quantity, special purpose work.

What is difference between comma and semi-colon (2 marks)
Answer:- (Page 8-163)
Comma ',' indicates that these two instructions are concurrent and only one of them would execute at a time. Comments are indicated by a semicolon (;) and can be placed anywhere in the source file. The FALSIM assembler ignores any text after the semicolon.

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1. **What is the difference between CPU Register and cache.**

Answer:- Rep

2. **How do you refer register in RTL .**

Answer:-Rep

3. **What are the advantages of RAID ?**

Answer:- (Page 329)
The main advantage of having an array of disks is that we could have a simultaneous I/O request. Latency could also be reduced..

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4. Give two advantages of virtual memory.
Answer:- Rep

5. Explain relationship between Hard disk , tracks , cylinders, sectors.
Answer:- Rep

6. Give difference between spatial Locality and Temporal correlatioin.
Answer:- Rep

7. Write about single server model and give example.
Answer:- (Page 381)
Consider a black box. Suppose it represents an I/O controller. At the input, we have arrival of different tasks. As one task is done, we have a departure at the output. So in the black box, we have a server. Now if we expand and open-up the black box, we could see that incoming calls are coming into the buffer and the output of the buffer is connected to the server. This is an example of "single server model".

8. Write structural RTL Call ra ,rb.
Answer:- (Page 165)

Step	RTL
T0-T2	Instruction Fetch
T3	C ← PC;
T4	R[ra] ← C;
T5	C ← R[rb];
T6	PC ← C;

10. Difference between Internal and external fragmentation.
Answer:- Rep

11. Give all steps of Integer division algorithm to divide 45 by 5 in 10 base systems.
Answer:- (Page 343)
There are steps of integer division present on page number 343 of course handouts. But none the less I am going to explain its working.

Divide 47 decimal with 5 decimal.

47 and 5 is converted into binary

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47 = 000000 101111

In this the left six bits are the upper half of dividend and the right ones are the lower half of the dividend.

5 = 000101

We use capital “D” for dividend and small “d” for divisor.

D = 000000 101111
d = 000101

First we shift left one bit the value of Dividend and add zero.

D = 0 000001 011110
d = 000101

(Now we if the result is negative than we append “0” to the quotient and if it is positive than we replace the upper half the dividend with the positive result and append “1” to the quotient.)

D = 0 000001 011110
d = 000101 q = 0

The result is negative so we append “0” to the quotient

D = 000010 111100
d = 000101 q = 00

The result is again negative so we append “0” to the quotient

D = 000101 111000
d = 000101

= 000000 q = 001

The result is positive so we append “1” to the quotient and replace the result with the upper half of the dividend.

Now D = 000000 111000

D = 000001 110000
d = 000101 q = 0010

The result is negative so we append “0” to the quotient

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D = 000011 100000
d = 000101 q = 00100

The result is again negative so we append “0” to the quotient

D = 000111 000000
d = 000101

= 000010 q = 001001

The result is positive so we append “1” to the quotient.

Remainder = 000010 = 2 decimal

Quotient = 001001 = 9 decimal

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2. An IO system with single disk gets 100 IO requests/sec. Assume the average time for a disk to service an IO request is 6ms. What is utilization of the IO system? (5)

Answer:- (Page 382)

Time for an I/O request = 6ms
=0.006sec
Server utilization = 100 x 0.006
= 0.6

3. What are characteristics of D-flip-flop? Draw truth table. (5)

Answer:- (Page 77)

A flip-flop is a bi-stable device, capable of storing one bit of Information. Therefore, flip-flops are used as the building blocks of a computer’s memory as well as CPU registers.
There are various types of flip-flops; most common type, the D flip-flop is shown in the figure given. The given truth table for this positive-edge triggered D flip-flop shows that the flip-flop is set (i.e. stores a 1) when the data input is high on the leading (also called the positive) edge of the clock; it is reset (i.e., the flip-flop stores a 0) when the data input is 0 on the leading edge of the clock. The clear input will reset the flip-flop on a low input.

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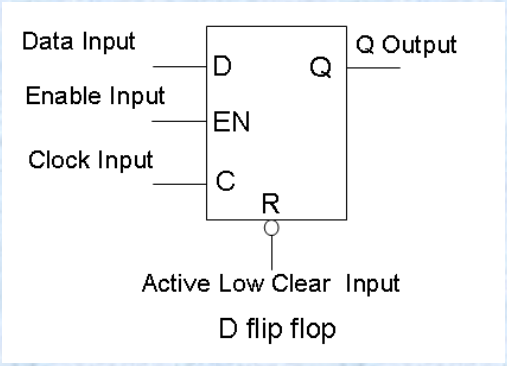

4. Does DMA affect the relationship b/w the memory system and CPU? Explain with reasons. (5)
Answer:- Rep

5. Diff b/w sender and receiver overhead related to network. (3)
Answer:- Rep

6. What are functions of valid bit in Associative mapping strategy for cache? (3)
Answer:- (Page 359)
A given block in cache is identified uniquely by its main memory block number, referred to as a tag, which is stored inside a separate tag memory in the cache. To check the validity of the cache blocks, a valid bit is stored for each cache entry, to verify whether the information in the corresponding block is valid or not.

7. Recode the integer 484 according to booth procedure. (3)
Answer:- Rep

8. Write structural RTL of ret ra. (3)
Answer:- (Page 165)

Step	RTL
T0-T2	Instruction Fetch
T3	C ← R[ra];
T4	PC ← C;

خاموشی غصے کا بہترین علاج ہے

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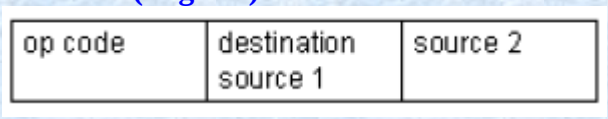
9. Consider a 64KB directed mapped cache with a line length of 32 bytes. Determine the number of bits in the address that refers to the byte within a cache line. (2)
Answer:- Rep

10. What attributes should a device have in order to be qualified as a master device? (2)
Answer:- Rep

11. What functions are provided by a typical memory cell? (2)
Answer:- Rep

12. What is format of 2-address instruction set? (2)
Answer:- (Page 35)



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1. Where is TCP/IP is used.
Answer:- Rep

2. Usage of DMA
Answer:- Rep

3. How to right RTL
Answer:- (Page 66)
RTL stands for Register Transfer Language. The Register Transfer Language provides a formal way for the description of the behavior and structure of a computer. The RTL facilitates the design process of the computer as it provides a precise, mathematical representation of its functionality. In this section, a Register Transfer Language is presented and introduced, for the SRC (Simple 'RISC' Computer), described in the previous discussion.

4. What you mean by ISA (Instruction Set Architecture)
Answer:- Rep

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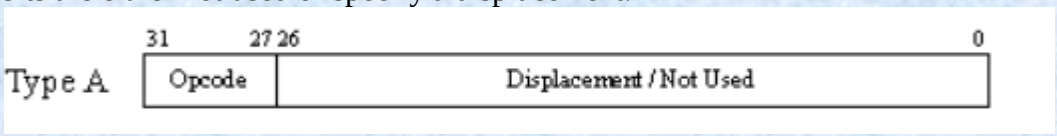
5. Define the different types of Instructions used in FALCON-E

Answer:- (Page 125)

Four different instruction formats are supported by the FALCON-E. These are

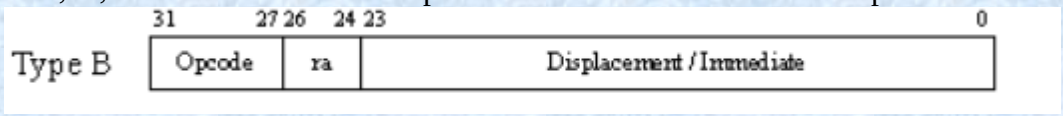
Type A instructions

The type A instructions have 5 bits reserved for the operation code (abbreviated op-code), and the rest of the bits are either not used or specify a displacement.



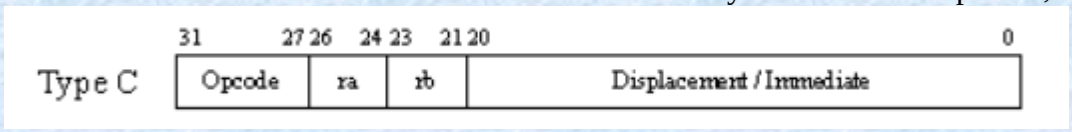
Type B instructions

The type B instructions also have 5 bits (27 through 31) reserved for the op-code. There is a register operand field, ra, and an immediate or displacement field in addition to the op-code field.



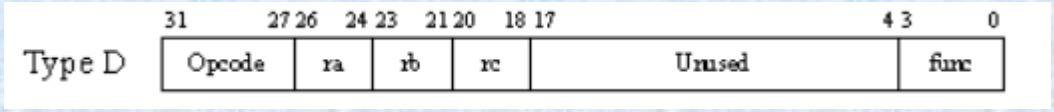
Type C instructions

Type C instructions have the 5-bit op-code field, two 3-bit operand registers (rb is the source register, ra is the destination register), a 17-bit immediate or displacement field, as well as a 3-bit function field. The function field is used to differentiate between instructions that may have the same op-code, but different operations.



Type D instructions

Type D instructions have the 5-bit op-code field, three 3-bit operand registers, 14 bits are unused, and a 3-bit function field.



6. Uni-bus interaction with I/O subsystem

8. Define one benefit and one Drawback of Cache.

Answer:- Rep

9. Define different level of RAID and What are the similarities at Level 2 and Level 3 of the RAID?

Answer:- (Page 329)

RAID Level 0

• Not a true member of the RAID family.
• Does not include redundancy to improve performance.
• In few applications, capacity and performance are primary concerns than improved reliability. So RAID level 0 is used in such applications.
• The user and system data are distributed across all the disks in the array.

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• Notable advantage over the use of a single large disk.
• Two requests can be issued in parallel, reducing the I/O queuing time.

Similarities between RAID Levels 2 and 3
• Make use of parallel access techniques.
• All member disks participate in execution of every request.
• Spindles of the individual drives are synchronized
• Data striping is used.
• Strips are as small as a single byte or word.

RAID Level 4
• Make use of independent access technique.
• Data striping is used.
• A bit-by-bit parity strip is calculated across corresponding strip on each data disk.
• Involves a write penalty when an I/O write request of small size is performed.
• To calculate the new parity, the array management software must read the old user parity strip.

RAID Level 5
• Organized in a similar fashion to RAID 4
• The only difference is that RAID 5 distributes the parity strips across all disks.

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Q1 (Marks: 5)
Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines
a) How many sets are there in the cache?
b) How many bits of address are required to select a set in cache?
Answer:- Rep

Q2 convert the hexadecimal number $B3_{16}$ to base 10 **5Marks**
Answer:- (Page 334)
According to the above algorithm,
X=0
X= x+B (=11) =11
X=16*11+3= 179
Hence $B3_{16}=179_{10}$

افضل انسان وہ ہے جو اپنی اصلاح کی کوشش کرتا ہے

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Q3 what do you know about " booth pair recording 3marks
Answer:- (Page 342)
The Booth Algorithm makes multiplication simple to implement at hardware level and speed up the procedure. This procedure is as follows:
1. Start with LSB and for each 0 of the original number, place a 0 in the recorded number until a 1 in indicated.
2. Place a 1 for 1in the recorded table and skip any succeeding 1's until a 0 is encountered.
3. Place a 0 with 1 and repeat the procedure.

Q.4 assembler symbol table note.3-marks:
Answer:-
Symbol table contains information to locate and relocate symbolic definitions and references. The assembler creates the symbol table section for the object file. It makes an entry in the symbol table for each symbol that is defined or referenced in the input file and is needed during linking.
Symbol Table corresponds to the storage of all program variables, labels and data values in a data structure at the implementation level. The Symbol Table includes data members, data addresses and labels with their respective values.

Q.5 configuration of 1x8 memory cell .3marks
Answer:- Rep

Q.6 Single detached DMA 5marks
Answer:- (Page 318)
When a particular I/O module needs to read or write large amounts contiguous data it requests the processor for direct memory access. If permission is granted by the processor, the I/O module sends the read or writes address and the size of data needed to be read or written to the DMA module. Once the DMA module acknowledges the request, the I/O module is free to read or write its contiguous block of data from or onto main memory. Even though in this situation the processor will not be able to execute while the transfer is going on (as there is a just a single bus to facilitate transfer of data), DMA transfer is much faster then having each word of memory being read by the processor and then being written to its location.

Q.7 what is hardisk 2 marks
Answer:- Rep

Q.8 difference bw connection oriented and connection less
Answer:- Rep

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Q1 what is assembler and what is it important in assembly language (2)
Answer:- Rep

Q2 what is program instruction control? (2)
Answer:- click here for detail
The program control instructions direct the flow of a program and allow the flow of the program to change. A change in flow often occurs when decisions, made with the CMP or TEST instruction, are followed by a conditional jump instruction.

Q3 define virtual memory (2)
Answer:- Rep

Q4 difference between higher level language and assembler (3)
Answer:- (Page 26)
Higher-level languages may not be appropriate for programming special purpose or embedded processors that are now in common use in various appliances. This is because the functionality required in such applications is highly specialized. In such a case, assembly language programming is required to implement the required functionality.

Q5define ISA
Answer:- Rep

Q6 convert (390)10 into base 16 (5)
Answer:- (Page 335)
According to the above algorithm
390/16 =24(rem=6), x0=6
24/16= 1(rem=8), x1=8, x2=1
Thus $390_{10}=186_{16}$

Q7 define pipelining(5)
Answer:- (Page 202)
Pipelining is a technique of overlapping multiple instructions in time. A pipelined processor issues a new instruction before the previous instruction completes. These results in a larger number of operations performed per unit of time. This approach also results in a more efficient usage of all the functional units present in the processor, hence leading to a higher overall throughput. As an example, many shorter integer instructions may be executed along with a longer floating point multiply instruction, thus employing the floating point unit simultaneously with the integer unit.

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Q8 define the type of error control(5)
Answer:- (Page 328)
There are two main issues in error control:
1. Detection of Error
2. Correction of Error
For detection of error, we just need to know that there exists an error. When the error is detected then the next step is to ask the source to resend that information. This process is called automatic request for repeat. In some cases there is also possibility that redundancy is enough and we reconstruct and find out exactly which particular bits are in error. This is called error correction.

Q9 define booth recording (2)
Answer:- Rep

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1. What is the purpose of control unit? 2
Answer:- Rep

2. Booth pair Recording? 2
Answer:- Rep

3. Which technique allows certain hardware subsystems within a computer to access system memory for read/write independently of the main CPU?
Answer:- click here for detail
Direct Memory Access. Allows certain hardware subsystems within a computer to access system memory for reading and/or writing independently of the main CPU. Examples of systems that use DMA: Hard Disk Controller, Disk Drive Controller, Graphics Card, Sound Card.

4. 64KB direct-mapped cache line length 32, determine number of bits in the address?
Answer:- Rep

5. Similarities and diff. between RAID level 4 and 5
Answer:- (Page 332)
RAID Level 4
• Make use of independent access technique.
• Data striping is used.
• A bit-by-bit parity strip is calculated across corresponding strip on each data disk.
• Involves a write penalty when an I/O write request of small size is performed.
• To calculate the new parity, the array management software must read the old user parity strip.

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RAID Level 5
• Organized in a similar fashion to RAID 4
• The only difference is that RAID 5 distributes the parity strips across all disks.

6. Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines
i. find sets in the cache
ii. and bit address required to select a set .
Answer:- Rep

7. Advantage of linker in the development of assembly language program
Answer:- Rep

8. Steps used for floating point addition and subtraction.
Answer:- (Page 00)
The following are the steps for floating-point addition and subtraction.
Unpack sign , exponent and fraction fields
Shift the significand
Perform addition
Normalize the sum
Round off the result
Check for overflow

9. Diff b/w distributed computing and computer Network and classifications of networks
Answer:- (Page 386)
Difference between Distributed Computing and Computer Networks
In distributed computing, all elements which are interconnected operate under one operating system. To a user, it appears as a virtual uni-processor system. In a computer network, the user has to specify and log in on a specific machine. Each machine on the network has a specific address. Different machines communicate by using the network which exists among them.
Classification of Networks
We can classify a network based on the following two parameters:
• The number and type of machines to be interconnected
• The distance between these machines

10.software polling and drawbacks of software polling and daisy chain
Answer:- (Page 283)
Software Poll
CPU polls to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt. This identification is done using special commands or reading the device status register. Special command may be a test I/O. In this case, CPU raises test I/O and places the address of a particular I/O module on the address line. If I/O module sets the interrupt then it responds positively. In the case of an addressable status register, the CPU reads the status register of each I/O module to identify the interrupting module. Once the correct module is identified, the CPU branches to a device service routine which is specific to that particular device.

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Disadvantages of Software Poll and Daisy Chain
The software poll has a disadvantage is that it consumes a lot of time, while the daisy chain is more efficient. The daisy chain has the disadvantage that the device nearest to the CPU would have highest priority. So, usually those devices which require higher priority would be connected nearer to the CPU. Now in order to get a fair chance for other devices, other mechanisms could be initiated or we could say that we could start instead of device 0 from that device where the CPU finishes the last interrupt and could have a cyclic provision to different devices.

11.cache and it's management
Answer:- Rep

12. compare RISC and CISC
Answer:- Rep

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What is DMA?
Answer:- Rep

Differentiate between throughput and latency?
Answer:- (Page 203)
Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second. Pipelining cannot lower the latency of a single instruction; however, it does increase the throughput. With respect to the example discussed earlier, in a non-pipelined machine there would be one instruction processed after an average of 5 cycles, while in a pipelined machine, instructions are completed after each and every cycle (in the steady-state, of course!!!). Hence, the overall time required to execute the program is reduced.

Describe six attributes of SRC Processor?
Answer:- (Page 46)
• The SRC contains 32 General Purpose Registers: R0, R1, …, R31; each register is of size 32-bits.
• Two special purpose registers are included: Program Counter (PC) and Instruction Register (IR)
• Memory word size is 32 bits
• Memory space size is 2^{32} bytes
• Memory organization is 2^{32} x 8 bits, this means that the memory is byte aligned
• Memory is accessed in 32 bit words (i.e., 4 byte chunks)
• Big-endian byte storage is used

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Briefly Describe Classification of Networks?
Answer:- (Page 387)
Classification of Networks
We can classify a network based on the following two parameters:
• The number and type of machines to be interconnected
• The distance between these machines
Based on these two parameters, we have the following type of networks:
SAN (System/Storage Area Network)
It refers to a cluster of machines where large disk arrays are present. Typical distances could be tens of meters.
LAN (Local Area Network)
It refers to the interconnection of machines in a building or a campus. Distances could be in Kilometers.
WAN (Wide Area Network)
It refers to the interconnection between LANs.

Write note on Pipelining?
Answer:- Rep

What is virtual memory?
Answer:- Rep

How does work Associative Mapping?
Answer:- (Page 359)
In this technique, block of data from main memory can be placed at any location in the cache memory. A given block in cache is identified uniquely by its main memory block number, referred to as a tag, which is stored inside a separate tag memory in the cache. To check the validity of the cache blocks, a valid bit is stored for each cache entry, to verify whether the information in the corresponding block is valid or not. Main memory address references have two fields. • The word field becomes a "cache address" which specifies where to find the word in the cache.
• The tag field which must be compared against every tag in the tag memory.

How overflow is represented in case of floating point?
Answer:- (Page 348)
e^= 255, denotes numbers with no numeric value including + ∞ and - ∞ and called Not-a-Number or NaN. In computers, a floating-point number ranges from 1.2 × 10-38 ≤ x ≤ 3.4 × 1038 can be represented. If a number does not lie in this range, then overflow can occur.
Overflow occurs when the exponent is too large and can not be represented in the exponent field.

ہر چیز کی ایک پہچان ہوتی ہے اور عقلمند کی پہچان غور و فکر کرنا ہے اور غور و فکر کی پہچان خاموشی ہے

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