	Fo	r More Visit <mark>VU Answer</mark>
	CS501 Fina	al Term Papers By Waqar (File 3)
	on No : 1 of 52	Marks: 1 (Budgeted Time 1 Mir
VV	/hat is the size of the memory space that is av	raliable to SRC processor?
swe	r (Please select your correct option)	VuAnswers.com
	2º bytes	
	2 ¹⁶ bytes	
	2 ³² bytes	<u>correct</u>
F	2 ⁶⁴ bytes	
2		Made by: Waqar Siddh
estic	on No : 2 of 52 /hich one of the following is the memory organ	Marks: 1 (Budgeted Time 1 Min
W		Marks: 1 (Budgeted Time 1 Min
W	/hich one of the following is the memory organ r (Please select your correct option)	Marks: 1 (Budgeted Time 1 Min
swe	hich one of the following is the memory organ r (Please select your correct option) 2° * 8 bits	Marks: 1 (Budgeted Time 1 Min
	hich one of the following is the memory organ r (Please select your correct option) 2* * 8 bits 2* * 8 bits 2* * 8 bits 2* * 8 bits	Marks: 1 (Budgeted Time 1 Min itzation of SRC processor? VuAnswers.com correct Marks: 1 (Budgeted Time 1 Min VuAnswers.com Siddb
swe	hich one of the following is the memory organ r (Please select your correct option) 2° * 8 bits 2° * 8 bits	Marks: 1 (Budgeted Time 1 Min itzation of SRC processor? VuAnswers.com correct Marks: 1 (Budgeted Time 1 Min VuAnswers.com Siddb
swe	hich one of the following is the memory organ r (Please select your correct option) 2° * 8 bits 2° * 8 bits	Marks: 1 (Budgeted Time 1 Mir itzation of SRC processor? VUAnswers.com correct
	hich one of the following is the memory organ r (Please select your correct option) 2° * 8 bits 2° * 8 bits	VuAnswers.com correct Made by: Wagar Siddh
	hich one of the following is the memory organ r (Please select your correct option) 2* * 8 bits 2* * 8 bits 0* No : 3 of 52 which one of the following addressing modes	Marks: 1 (Budgeted Time 1 Mir ization of SRC processor? VUAnswers.com correct Correct Marks: 1 (Budgeted Time 1 Mir s, the value to be stored in memory is obtained by directly retrieving it from another memory location?
swee	hich one of the following is the memory organ r (Please select your correct option) 2° * 8 bits 2° * 8 bits r (Please select your correct option)	Marks: 1 (Budgeted Time 1 Mir itzation of SRC processor? VuAnswers.com correct Marks: 1 (Budgeted Time 1 Mir State by: Magar Siddh Marks: 1 (Budgeted Time 1 Mir State by: 1 (Budgeted Time 1 Mir Marks: 1 (Budgeted Time 1 Mir State by directly retrieving it from another memory location? VuAnswers.com
weeking a sweeking a s	hich one of the following is the memory organ r (Please select your correct option) 2° * 8 bits 2° * 8 bits r (Please select your correct option) Direct Addressing Mode	Marks: 1 (Budgeted Time 1 Mir itzation of SRC processor? VuAnswers.com correct Marks: 1 (Budgeted Time 1 Mir State by: Magar Siddh Marks: 1 (Budgeted Time 1 Mir State by: 1 (Budgeted Time 1 Mir Marks: 1 (Budgeted Time 1 Mir State by directly retrieving it from another memory location? VuAnswers.com

rator is used to 'name' registers, or part of registers, in ase select your correct option) : 5 of 52 of the following register holds the address of the next in ase select your correct option)	vuAnswers.com correct Made by: Wagar Siddh Marks: 1 (Budgeted Time 1 Mi
: 5 of 52 of the following register holds the address of the next in ase select your correct option)	correct Made by: Wagar Siddh Marks: 1 (Budgeted Time 1 Mi
: 5 of 52 of the following register holds the address of the next in ase select your correct option)	correct Made by: Wagar Siddh Marks: 1 (Budgeted Time 1 Mi
of the following register holds the address of the next in ase select your correct option)	Made by: Waqar Siddh Marks: 1 (Budgeted Time 1 Mi
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of the following register holds the address of the next in ase select your correct option)	Marks: 1 (Budgeted Time 1 Mi
of the following register holds the address of the next in ase select your correct option)	Marks: 1 (Budgeted Time 1 Mi
of the following register holds the address of the next in ase select your correct option)	
ase select your correct option)	nstruction to be executed?
	VuAnswers.com
nulator	
ss Mask	
tion Register	
am Counter	
	meet Made by: Waqar Siddh
: 6 of 52	Marks: 1 (Budgeted Time 1 Mi
of the following register holds the instruction that is bein	ng executed?
ase select your correct option)	VuAnswers.com
nulator	
ss Mask	
tion Register	correct
am Counter	
1	ion Register m Counter 6 of 52 of the following register holds the instruction that is bei asse select your correct option) ulator ass Mask

ion No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
h one of the following is the highest level of abstraction in digital design	in which the computer architect views the system for the description of system components and their interconnections?
er (Please select your correct option)	VuAnswers.com
Processor-Memory-Switch level (PMS level)	correct
nstruction Set Level	
Register Transfer Level	
.ogic design level	Made by: Waqar Siddhu
ion No : 8 of 52	Marks: 1 (Budgeted Time 1 Min)
r (Please select your correct option)	VuAnswers.com
Logic Design Level	correct
Circuit Level	
Mask Level	
Register transfer Level	Made by: Waqar Siddhu
Register transfer Level	Marks: 1 (Budgeted Time 1 Min)
	Marks: 1 (Budgeted Time 1 Min)
on No : 9 of 52 Instructions usually involve calculating the target address and e	Marks: 1 (Budgeted Time 1 Min)
on No : 9 of 52 Instructions usually involve calculating the target address and e r (Please select your correct option)	Marks: 1 (Budgeted Time 1 Min)
on No : 9 of 52 Instructions usually involve calculating the target address and e er (Please select your correct option) Add	Marks: 1 (Budgeted Time 1 Min)
on No : 9 of 52 Instructions usually involve calculating the target address and e er (Please select your correct option) Add Branch	Marks: 1 (Budgeted Time 1 Min) evaluating a condition. VuAnswers.com
ion No : 9 of 52	Marks: 1 (Budgeted Time 1 Min) evaluating a condition. VuAnswers.com

Í	tion No : 10 of 52	Marks: 1 (Budgeted Time 1 Min
nic	ch one of the following instructions is used to load register from memory using a relative address?	
swe	rer (Please select your correct option)	VuAnswers.com
2	la	
F	nop	
	ldr correct	
L	str	
		Made by: Waqar Siddh
	tion No : 11 of 52	Marks: 1 (Budgeted Time 1 Min
ım	nterface that is used to connect the computer bus with I/O devices is called	
Г	er (Please select your correct option)	VuAnswers.com
-	rer (Please select your correct option) Buffer	VuAnswers.com
	Buffer	VuAnswers.com
		VuAnswers.com
	Buffer I/O port	VuAnswers.com
	Buffer I/O port	VuAnswers.com
	Buffer I/O port	VuAnswers.com
	Buffer I/O port Memory mapping Processor	VuAnswers.com Made by: Wagar Siddh
	Buffer I/O port Memory mapping Processor	
esti	Buffer I/O port Memory mapping Processor	Made by: Maqar Siddh
esti	Buffer I/O port Memory mapping Processor tion No : 12 of 52	Made by: Maqar Siddh
esti	Buffer I/O port Memory mapping Processor tion No : 12 of 52	Made by: Maqar Siddh
esti very	Buffer I/O port Memory mapping Processor tion No : 12 of 52	Made by: Maqar Siddh
esti	Buffer J/O port Correct Memory mapping Processor f too No : 12 of 52 y J/O port has a unique identifier associated with it, which is called its ter (Please select your correct option) Address	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
esti	Buffer J/O port Correct Memory mapping Processor (ton No : 12 of 52 y J/O port has a unique identifier associated with it, which is called its rer (Please select your correct option)	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
esti	Buffer J/O port Correct Memory mapping Processor f too No : 12 of 52 y J/O port has a unique identifier associated with it, which is called its ter (Please select your correct option) Address	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
	Buffer I/O port CONSCI Memory mapping Processor (tion No : 12 of 52 y I/O port has a unique identifier associated with it, which is called its rer (Please select your correct option) Address CONSCI Access point	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
esti	Buffer J/O port Correct Memory mapping Processor f tion No : 12 of 52 y J/O port has a unique identifier associated with it, which is called its ter (Please select your correct option) Address Correct	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
	Buffer J/O port Correct Memory mapping Processor for No : 12 of 52 y J/O port has a unique identifier associated with it, which is called its rer (Please select your correct option) Address Correct Access point Interval Identifier	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
	Buffer J/O port Correct Memory mapping Processor (tion No : 12 of 52 y J/O port has a unique identifier associated with it, which is called its rer (Please select your correct option) Address Correct Access point Interval Identifier Device driver	Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min

ver (Please select your correct option)		VuAn	swers.com
Direct memory access			
Virtual memory			
Partial decoding			
Programmed I/O	correct	Made by:	Waqar Siddhu
tion No : 14 of 52		<u> </u>	Marks: 1 (Budgeted Time 1 Min)
is the process of periodically checking the s	tatus of a device to see if it is ready for the n	ext I/O operation.	
		VuAp	swers.com
er (Please select your correct option) Polling		VUAII	Sweis.com
	<u>correct</u>		
Snooping			
Data Bus Multiplexing			
Data Dus Humplexing			
Pipelining		044 I I	
		(VY)ade by:	Waqar Siddhu
tion No : 15 of 52	he CPU wants to exchange data with periph	eral device?	Marks: 1 (Budgeted Time 1 Min)
ch one of the following is NOT a technique used when t			
:h one of the following is \mathbf{NOT} a technique used when t			
:h one of the following is \mathbf{NOT} a technique used when t			
		VuAn	swers.com
er (Please select your correct option)		VuAn	swers.com
er (Please select your correct option) Direct Memory Access		VuAn	swers.com
er (Please select your correct option) Direct Memory Access		VuAn	swers.com
er (Please select your correct option) Direct Memory Access Interrupt driven I/O		VuAn	swers.com
er (Please select your correct option) Direct Memory Access Interrupt driven I/O Programmed I/O		VuAn	swers.com
ch one of the following is NOT a technique used when t er (Please select your correct option) Direct Memory Access Interrupt driven I/O Programmed I/O Virtual Memory	correct		
er (Please select your correct option) Direct Memory Access Interrupt driven I/O Programmed I/O	correct		swers.com
er (Please select your correct option) Direct Memory Access Interrupt driven I/O Programmed I/O	correct		

For More V	
ion No : 16 of 52	Marks: 1 (Budgeted Time 1 Min)
h one is the last instruction of the ISR that is to be executed when the ISR termin	lates?
r (Please select your correct option) RET	VuAnswers.com
	contect
RQ	
NT	
n <i>a</i>	
IMI	Made by: Waqar Siddhu
on No : 17 of 52	Marks: 1 (Budgeted Time 1 Min)
is the time needed by the CPU to recognize (not service) an interrupt r	equest.
r (Please select your correct option)	VuAnswers.com
nterrupt Latency	
	correct
Response Deadline	
Fimer delay	
Throughput	
erre contribute	Made by: Waqar Siddhu
on No : 18 of 52	Marks: 1 (Budgeted Time 1 Min)
ltiple Interrupt Lines approach, a number of interrupt lines are provided betwee	n the modules.
r (Please select your correct option)	VuAnswers.com
External and Internal	
CPU and I/O	conrect
CPU and Memory	
P O and Memory	
and the restation are approved at the	
2	
-	Made by: Waqar Siddhu
-	Made by: Waqar Siddhu
2	Made by: Waqar Siddhu
2	Made by: Waqar Siddhu
2	Made by: Waqar Siddhu
Memory and I/O	Made by: Waqar Siddhu
2	Made by: Waqar Siddhu

tion No : 19 of 52	Marks: 1 (Budgeted Time 1 Min)
	and presents its contents into different areas of the simulator.
er (Please select your correct option)	VuAnswers.com
bin	
binfa	correct
.fa	
asmfa	
tion No : 20 of 52	Made by: Waqar Siddhu
tion No : 20 of 52 irect memory access (DMA), a is needed to control the total act	Marks: 1 (Budgeted Time 1 Min)
er (Please select your correct option)	VuAnswers.com
DMA memory unit	VU/TIGWCIG.COTT
DMA controller	
a	<u>correct</u>
Control software	
Programmed I/O	
	Made by: Waqar Siddhu
tion No : 21 of 52	Marks: 1 (Budgeted Time 1 Min)
allows a peripheral device to read from and/or write to memor	y without intervention by the CPU.
	VuAnswers.com
	VuAnswers.com
Programmed I/O	VuAnswers.com
Programmed I/O Interrupt driven I/O	VuAnswers.com
Programmed I/O Interrupt driven I/O Direct memory access	VuAnswers.com
Programmed I/O Interrupt driven I/O Direct memory access	
rer (Please select your correct option) Programmed I/O Interrupt driven I/O Direct memory access Polling	correct
Programmed I/O Interrupt driven I/O Direct memory access	correct
Programmed I/O Interrupt driven I/O Direct memory access	correct
Programmed I/O Interrupt driven I/O Direct memory access	correct
Programmed I/O Interrupt driven I/O Direct memory access	
Programmed I/O Interrupt driven I/O Direct memory access	zorrect

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Marks: 1 (Budgeted Time 1 Min)
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Marks: 1 (Budgeted Time 1 Min)
VuAnswers.com
Made by: Waqar Siddh

	tion No : 25 of 52	Mades 4 (Dudgets d Time 4 Min)
	tion No : 25 of 52 represent e^ instead of e to show	Marks: 1 (Budgeted Time 1 Min)
14	ver (Please select your correct option)	VuAnswers.com
3	Sign Magnitude Form	
	Radix Complement Form	
	Diminished Radix Compliment Form	
	Biased Representation	
1000	correct	Made by: Waqar Siddhu
les	tion No : 26 of 52	Marks: 1 (Budgeted Time 1 Min)
ц	oating point representations is also called mantissa.	
sw	rer (Please select your correct option)	VuAnswers.com
,	Sign	
	Base	
	Significand	
	correct	
	Exponent	
	Exponent	Made bu: Magar Siddhu
	tion No : 27 of 52	Made by: Waqar Siddhu Marks: 1 (Budgeted Time 1 Min)
		Marks: 1 (Budgeted Time 1 Min)
	tion No : 27 of 52	Marks: 1 (Budgeted Time 1 Min)
	tion No : 27 of 52	Marks: 1 (Budgeted Time 1 Min)
	tion No : 27 of 52	Marks: 1 (Budgeted Time 1 Min)
es	tion No : 27 of 52	Marks: 1 (Budgeted Time 1 Min)
es	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field	Marks: 1 (Budgeted Time 1 Min)
	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field rer (Please select your correct option)	Marks: 1 (Budgeted Time 1 Min)
es sw	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field rer (Please select your correct option) Underflow Overflow	Marks: 1 (Budgeted Time 1 Min)
sw	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field rer (Please select your correct option) Underflow	Marks: 1 (Budgeted Time 1 Min)
BS SW	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field rer (Please select your correct option) Underflow Overflow	Marks: 1 (Budgeted Time 1 Min)
BS SW	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field rer (Please select your correct option) Underflow Overflow	Marks: 1 (Budgeted Time 1 Min)
sw	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field rer (Please select your correct option) Underflow Overflow	Marks: 1 (Budgeted Time 1 Min) I. VuAnswers.com
:w	tion No : 27 of 52 occurs when the exponent is too large and can not be represented in the exponent field ver (Please select your correct option) Underflow Overflow Correct Rounding Off	L

stion No : 28 of 52	Marks: 1 (Budgeted Time 1 Min)
Double-Precision Binary Floating Point Representation the si	ize of fraction is
wer (Please select your correct option)	VuAnswers.com
52-bits	correct
1-bits	Made by: Waqar Siddhu
stion No : 29 of 52	Marks: 1 (Budgeted Time 1 Min)
is a combination of arithmetic, logic and shifter unit al	
wer (Please select your correct option)	VuAnswers.com
Computer Bus	
CPU Register	
Flip Flop	
ALU	
	correct Made by: Wagar Siddhu
stion No : 30 of 52	Marks: 1 (Budgeted Time 1 Min)
is a place for safe storage and provides the fastest po	ssible storage atter the registers.
wer (Please select your correct option)	VuAnswers.com
Hard Disk	
	correct
Cache	
Cache Compact Disk	
Compact Disk	Made by: Waqar Siddhu
Compact Disk.	
Compact Disk.	
Compact Disk.	
Compact Disk	

	Marks: 1 (Budgeted Time 1 Min
is nonvolatile i.e. it retains the information in it when power is removed from it.	
er (Please select your correct option)	VuAnswers.com
RAM	
DRAM	
ROM	±
SRAM	
	Made by: Waqar Siddh
ion No : 32 of 52	Marks: 1 (Budgeted Time 1 Min
d on the statistical results, the cache block which has been least used in the recent past, is	replaced with a new block. This technique is called
er (Please select your correct option) Always Replacement	VuAnswers.com
	VuAnswers.com
	VuAnswers.com
Always Replacement	VuAnswers.com
Always Replacement Random Replacement LFU (Least Frequently Used)	VuAnswers.com
Always Replacement Random Replacement LFU (Least Frequently Used)	
Always Replacement Random Replacement LFU (Least Frequently Used)	
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate	rect
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate	rect Made by: Magar Siddh
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate	rect Made by: Magar Siddh
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate ion No : 33 of 52acts as a cache between main memory and secondary memory.	rect Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate	rect Made by: Magar Siddh
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate ion No : 33 of 52acts as a cache between main memory and secondary memory. art Please select your correct option)	rect Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate ion No : 33 of 52acts as a cache between main memory and secondary memory. art Please select your correct option)	rect Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate ion No : 33 of 52 acts as a cache between main memory and secondary memory. ar (Please select your correct option) Read Only Memory Flash Memory	rect Made by: Magar Siddh Marks: 1 (Budgeted Time 1 Min
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate ion No : 33 of 52 acts as a cache between main memory and secondary memory. art Please select your correct option Read Only Memory	Tect Marks: 1 (Budgeted Time 1 Min VuAnswers.com
Always Replacement Random Replacement LFU (Least Frequently Used) Write Allocate ion No : 33 of 52 acts as a cache between main memory and secondary memory. er (Please select your correct option) Read Only Memory Flash Memory Virtual Memory	Tect Marks: 1 (Budgeted Time 1 Min VuAnswers.com

on No : 34 of 52				Marks: 1 (Budgeted Time 1 Min)
technique memory is divided into segments of variable sizes depen	nding upon the requirements.			
r (Please select your correct option)		Vu,	Answers.	com
Aultiplexing				
egmentation				
	correct			
Iamming code				
'artial decoding				and the second second
		Made b	y: W	aqar Siddhu
on No : 35 of 52				Marks: 1 (Budgeted Time 1 Min)
is the maximum rate at which data can be transmitted through network	.8.			
r (Please select your correct option)		Vu	Answers.	com
ransmission Time				
atency				
ransport Latency				
andwidth				
	correct	Made b	9: W	agar Siddhu
on No : 36 of 52 sical media of networks, for increased and better performance we use	which are usually made of glass	7		Marks: 1 (Budgeted Time 1 Min)
(Please select your correct option)		Vu	Answers.	com
oaxial Cables				
wisted Pair Cables				
ber Optic Cables				
	<u>correct</u>			
hielded Twisted Pair Cables		MA 1-1		0.111
		and a second	y: W	aqar Siddhu

	on No : 37 of 52	Marks: 1 (Budgeted Time 1 Min)
	topology, all the computers are connected in the form of a circle.	
1	(Please select your correct option)	VuAnswers.com
в	us-	
R	ing correct	
N		
S	tar	Made has Selecter Ciddle
estic	vn No : 38 of 52	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
	ction Oriented Communication reserves the until the transfer is completed.	marks - Loadgeled Time - Mini
swer	(Please select your correct option)	VuAnswers.com
В	andwidth	VuAnswers.com
В	andwidth correct	VuAnswers.com
B	andwidth	VuAnswers.com
E	andwidth correct	VuAnswers.com
	andwidth rror hecksum	VuAnswers.com
	andwidth correct	
	andwidth rror hecksum	VuAnswers.com
E C P	andwidth conoct rror hecksum rotocol	Made by: Waqar Siddhu
E C P	andwidth rror hecksum rotocol n No : 39 of 52	Made by: Waqar Siddhu
E C P estic	andwidth rror hecksum rotocol n No : 39 of 52	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
B C P com	andwidth rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into	Made by: Waqar Siddhu
E C P com swer	andwidth rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
B C P com	andwidth rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
B C P com	andwidth rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into (Please select your correct option) racks	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
E C P com	andwidth rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into (Please select your correct option) racks	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
B E C C P C C C C C C C C C C C C C C C C	andwidth rror rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into (Please select your correct option) racks ectors latters	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)
B C P com	andwidth rror hecksum rotocol n No : 39 of 52 nection-less communication message is divided into (Please select your correct option) racks ectors	Made by: Magar Siddhu Marks: 1 (Budgeted Time 1 Min)

er (Please click here to Add Answer)	tion No : 40 of 52	Marks: 1 (Budgeted Time 1 Min)
ESC SEC SEC SEC SEC SEC SEC SEC	RC (Scalable Processor Architecture) is an example ofarchitecture.	
SEC		
SEC		
set FALCOM FALCO		vuAnswers.com
set FALCOM FALCO		
SRC FALCON FALCON FALCON FALCON FALCON FALCON (Please click here to Add Answer) F(Please click		
ALCOM AND IN 19 AND	й	
Market by: Market Sided into it it to to entities between Latency and throughput. into it it to to into it it to to into it it to to into it it to into it it to to into it it to to into it it to into it it to into it it it to into it it it to into it		
In No : 41 of 52 Marke: 2 (Budgeted Time 4 entities between Latency and throughput. VUAnswers.com Image: Comparison of the comparison o	FALCON	Mada hu Jalaaan fiddhu
erritate between Latency and throughput. ar (Please glick here to Add Answer) VuAnswers.com Latency is defined as the time required to process a single instruction, while throughput isdefined as the number of instructions processed per second Marke: 2 (Budgeted Time 4 h attributer a device should have in order to be qualified as a matter device? Master must have the capability to place addresses on the ddress bus and direct the bus activity during a buscycle	ion No : 41 of 52	Marks: 2 (Budgeted Time 4 Min)
Latency is defined as the time required to process a single instruction, while throughput isdefined as the number of instructions processed per second More : 42 of 52 Marke: 2 (Budgeted Time 4 h attrbutes a device should have in order to be qualified as a master device? Marker must have the capability to place addresses on the ddress bus and direct the bus activity during a buscycle	entiate between Latency and throughput.	 Construction of the second s Second second se Second second s
Latency is defined as the time required to process a single instruction, while throughput isdefined as the number of instructions processed per second More 20 Marker Sidda Marker to be qualified as a master device? Marker to Add Answer VuAnswers.com Master must have the capability to place addresses on the ddress bus and direct the bus activity during a buscycle		
Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second More 20 Marker Sidda Marker 2 (Budgeted Time 4 hattrbutes a device should have in order to be qualified as a master device? Marker to Add Answer VuAnswers.com Master must have the capability to place addresses on the ddress bus and direct the bus activity during a buscycle		
Latency is defined as the time required to process a single instruction, while throughput isdefined as the number of instructions processed per second More 20 10 Marker 2 (Budgeted Time 4 A attributes a device should have in order to be qualified as a master device? Marker 2 (Budgeted Time 4 A attributes a device should have in order to be qualified as a master device? Marker 2 (Budgeted Time 4 A attributes a device should have in order to be qualified as a master device? Marker 2 (Budgeted Time 4 A attributes a device should have in order to be qualified as a master device? Marker 2 (Budgeted Time 4 A attributes a device should have in order to be qualified as a master device? Marker was that the capability to place addresses on the ddress bus and direct the bus activity during a buscycle	r(Please <u>click here</u> to Add Answer)	VuAnswers.com
Latency is defined as the time required to process a single instruction, while throughput isdefined as the number of instructions processed per second		
h attributes a device should have in order to be qualified as a master device? Tr (Please click here to Add Answer) VuAnswers.com Image: Second Add Answer) Image: Second Add Add Add Add Add Add Add Add Add	second	uctions processed per
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stion No : 46 of 52	Marks: 3 (Budgeted Time 6 Min)
te down the categories of instructions supported by FALCON-A processor and also state that in typ	e 1 instruction format of FALCON-A, how many bits are reserved for the op-code?
rer (Please <u>click here</u> to Add Answer)	VuAnswers.com
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tion No : 47 of 52	Made by: Wagar Siddhu Marks: 3 (Budgeted Time 6 Min)
I the average rotational latency (in milliseconds) of the disk if it rotates at 15,000 rpm.	
ver (Please <u>click here</u> to Add Answer)	VuAnswers.com
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	Made by: Wagar Siddhu Marks: 3 (Budgeted Time 6 Min)
tion No : 48 of 52	Marks: 3 (Budgeted Time 6 Min)
stion No : 48 of 52	Marks: 3 (Budgeted Time 6 Min)
tion No : 48 of 52 DRAM has 512 rows and its refresh time is 8ms, what should be the average frequency of row refre rer (Please click here to Add Answer)	Marks: 3 (Budgeted Time 6 Min)
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iestion No : 49 of 52	Marks: 5 (Budgeted Time 10 Mir
riefly explain the following features of FALCON-E.	
a. Number of registers	
 b. Size of each register c. Memory word size 	
d. Memory space	
nswer (Please <u>click here</u> to Add Answer)	VuAnswers.com
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Investion No : 50 of 52 Explain briefly how the interrupting module is identified in software polling and also point out the majo Inswer (Please click here to Add Answer) Image: Second Seco	Marks: 5 (Budgeted Time 10 Mir r drawback of Software Poll and Daisy Chain.
Explain briefly how the interrupting module is identified in software polling and also point out the majo newer (Please <u>click here</u> to Add Answer)	Marks: 5 (Budgeted Time 10 Mir r drawback of Software Poll and Daisy Chain.
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uestion No : 51 of 52	Marks: 5 (Budgeted Time 10 Min)
ccording to the Radix conversion algorithm, convert the hexadecimal numb	ber C416 to base 10 (Write down all the steps which are involved in conversion).
nswer (Please <u>click here</u> to Add Answer)	VuAnswers.com
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uestion No : 52 of 52	Marks: 5 (Budgeted Time 10 Min)
Juestion No : 52 of 52 Find the average access time of a level of memory hierarchy if the hit rate is	Marks: 5 (Budgeted Time 10 Min)
uestion No : 52 of 52 Find the average access time of a level of memory hierarchy if the hit rate is	Marks: 5 (Budgeted Time 10 Min) 80%. The memory access takes 10ns on a hit and 100ns on a miss. VuAnswers.com
Aussetion No : 52 of 52 Find the average access time of a level of memory hierarchy if the hit rate is Answer (Please click here to Add Answer) Image: Source of the second sec	Marks: 5 (Budgeted Time 10 Min) 80%. The memory access takes 10ns on a hit and 100ns on a miss. VuAnswers.com