CS501 Final Term Papers By Waqar (File 3)

Question No : 1 of 52 Marks: 1 (Budgeted Time 1 Min)

What is the size of the memory space that is available to **SRC processor?**

Answer (Please select your correct option)

- 2^8 bytes
- 2^{16} bytes
- 2^{32} bytes

correct

- 2^{64} bytes

Question No : 2 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following is the memory organization of **SRC processor?**

Answer (Please select your correct option)

- 2^8 * 8 bits
- 2^{16} * 8 bits
- 2^{32} * 8 bits

correct

- 2^{64} * 8 bits

Question No : 3 of 52 Marks: 1 (Budgeted Time 1 Min)

In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

Answer (Please select your correct option)

- Direct Addressing Mode

correct

- Immediate addressing mode
- Indirect Addressing Mode
- Register (Direct) Addressing Mode

Question No : 4 of 52 Marks: 1 (Budgeted Time 1 Min)

Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

Answer (Please select your correct option)

- := correct
- &
- %
- ©

Question No : 5 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following register holds the address of the next instruction to be executed?

Answer (Please select your correct option)

- Accumulator
- Address Mask
- Instruction Register
- Program Counter correct

Question No : 6 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following register holds the instruction that is being executed?

Answer (Please select your correct option)

- Accumulator
- Address Mask
- Instruction Register correct
- Program Counter

For More Visit VU Answer

Question No : 7 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

Answer (Please select your correct option)

- Processor-Memory-Switch level (PMS level) correct
- Instruction Set Level
- Register Transfer Level
- Logic design level

Question No : 8 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following design levels is called the gate level?

Answer (Please select your correct option)

- Logic Design Level correct
- Circuit Level
- Mask Level
- Register transfer Level

Question No : 9 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ Instructions usually involve calculating the target address and evaluating a condition.

Answer (Please select your correct option)

- Add
- Branch correct
- Load
- Store

Question No : 10 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following instructions is used to load register from memory using a relative address?

Answer (Please select your correct option)

- la
- nop
- ldr

correct

- str

Question No : 11 of 52 Marks: 1 (Budgeted Time 1 Min)

An interface that is used to connect the computer bus with I/O devices is called _____.

Answer (Please select your correct option)

- Buffer
- I/O port

correct

- Memory mapping
- Processor

Question No : 12 of 52 Marks: 1 (Budgeted Time 1 Min)

Every I/O port has a unique identifier associated with it, which is called its ----------

Answer (Please select your correct option)

- Address

correct

- Access point
- Interval Identifier
- Device driver

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Question No : 13 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ refers to the situation in which all I/O operations are performed under the direct control of a program running on the CPU.

Answer (Please select your correct option)

- Direct memory access
- Virtual memory
- Partial decoding
- Programmed I/O

correct

Question No : 14 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is the process of periodically checking the status of a device to see if it is ready for the next I/O operation.

Answer (Please select your correct option)

- Polling

correct

- Snooping
- Data Bus Multiplexing
- Pipelining

Question No : 15 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following is **NOT** a technique used when the CPU wants to exchange data with peripheral device?

Answer (Please select your correct option)

- Direct Memory Access
- Interrupt driven I/O
- Programmed I/O
- Virtual Memory

correct

Question No : 16 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

Answer (Please select your correct option)

- IRET correct
- IRQ
- INT
- NMI

Question No : 17 of 52 Marks: 1 (Budgeted Time 1 Min)

---------- is the time needed by the CPU to recognize (not service) an interrupt request.

Answer (Please select your correct option)

- Interrupt Latency correct
- Response Deadline
- Timer delay
- Throughput

Question No : 18 of 52 Marks: 1 (Budgeted Time 1 Min)

In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

- External and Internal
- CPU and I/O correct
- CPU and Memory
- Memory and I/O

For More Visit VU Answer

Question No : 19 of 52 Marks: 1 (Budgeted Time 1 Min)

Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.

Answer (Please select your correct option)

- .bin
- .binfa
  correct
- .fa
- .asmfa

Question No : 20 of 52 Marks: 1 (Budgeted Time 1 Min)

In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

Answer (Please select your correct option)

- DMA memory unit
- DMA controller
  correct
- Control software
- Programmed I/O

Question No : 21 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

Answer (Please select your correct option)

- Programmed I/O
- Interrupt driven I/O
- Direct memory access
  correct
- Polling

For More Visit VU Answer

Question No : 22 of 52 Marks: 1 (Budgeted Time 1 Min)

Taking control of the system bus for a few bus cycles is known as _____.

Answer (Please select your correct option)

- Bus Scheduling
- Cycle Stealing — correct
- Cycle Transferring
- CPU Scheduling

Question No : 23 of 52 Marks: 1 (Budgeted Time 1 Min)

A component connected to the system bus and having control of it during a particular bus cycle is called _____.

Answer (Please select your correct option)

- Address decoder
- BIOS
- Master component — correct
- Slave component

Question No : 24 of 52 Marks: 1 (Budgeted Time 1 Min)

CRC has _____overhead as compared to Hamming code.

Answer (Please select your correct option)

- Equal
- Greater
- Lesser — correct
- Absolutely no

For More Visit VU Answer

Question No : 25 of 52 Marks: 1 (Budgeted Time 1 Min)

We represent e^ instead of e to show_____.

Answer (Please select your correct option)

- Sign Magnitude Form
- Radix Complement Form
- Diminished Radix Compliment Form
- Biased Representation

correct

Question No : 26 of 52 Marks: 1 (Budgeted Time 1 Min)

In floating point representations _____ is also called mantissa.

Answer (Please select your correct option)

- Sign
- Base
- Significand

correct

- Exponent

Question No : 27 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ occurs when the exponent is too large and can not be represented in the exponent field.

Answer (Please select your correct option)

- Underflow
- Overflow

correct

- Rounding Off
- Normalization

For More Visit VU Answer

Question No : 28 of 52 Marks: 1 (Budgeted Time 1 Min)

In Double-Precision Binary Floating Point Representation the size of fraction is _____.

Answer (Please select your correct option)

- 23-bits
- 52-bits correct
- 11-bits
- 1-bits

Question No : 29 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers.

Answer (Please select your correct option)

- Computer Bus
- CPU Register
- Flip Flop
- ALU correct

Question No : 30 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is a place for safe storage and provides the fastest possible storage after the registers.

Answer (Please select your correct option)

- Hard Disk
- Cache correct
- Compact Disk
- Floppy Disk

Question No : 31 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is nonvolatile i.e. it retains the information in it when power is removed from it.

Answer (Please select your correct option)

- RAM
- DRAM
- ROM

correct

- SRAM

Question No : 32 of 52 Marks: 1 (Budgeted Time 1 Min)

Based on the statistical results, the cache block which has been least used in the recent past, is replaced with a new block. This technique is called _____.

Answer (Please select your correct option)

- Always Replacement
- Random Replacement
- LFU (Least Frequently Used)

correct

- Write Allocate

Question No : 33 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ acts as a cache between main memory and secondary memory.

Answer (Please select your correct option)

- Read Only Memory
- Flash Memory
- Virtual Memory

correct

- Magnetic Tape

Question No : 34 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____technique memory is divided into segments of variable sizes depending upon the requirements.

Answer (Please select your correct option)

- Multiplexing
- Segmentation

correct

- Hamming code
- Partial decoding

Question No : 35 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is the maximum rate at which data can be transmitted through networks.

Answer (Please select your correct option)

- Transmission Time
- Latency
- Transport Latency
- Bandwidth

correct

Question No : 36 of 52 Marks: 1 (Budgeted Time 1 Min)

In physical media of networks, for increased and better performance we use _____ which are usually made of glass.

Answer (Please select your correct option)

- Coaxial Cables
- Twisted Pair Cables
- Fiber Optic Cables

correct

- Shielded Twisted Pair Cables

For More Visit VU Answer

Question No : 37 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____ topology, all the computers are connected in the form of a circle.

Answer (Please select your correct option)

- Bus
- Ring correct
- Mesh
- Star

Question No : 38 of 52 Marks: 1 (Budgeted Time 1 Min)

Connection Oriented Communication reserves the _____ until the transfer is completed.

Answer (Please select your correct option)

- Bandwidth correct
- Error
- Checksum
- Protocol

Question No : 39 of 52 Marks: 1 (Budgeted Time 1 Min)

In connection-less communication message is divided into _____.

Answer (Please select your correct option)

- Tracks
- Sectors
- Platters
- Packets correct

Question No : 40 of 52 Marks: 1 (Budgeted Time 1 Min)

SPARC (Scalable Processor Architecture) is an example of _____architecture.

Answer (Please select your correct option)

- CISC
- RISC

correct

- SRC
- FALCON

Question No : 41 of 52 Marks: 2 (Budgeted Time 4 Min)

Differentiate between Latency and throughput.

Answer (Please click here to Add Answer)

Latency is defined as the time required to process a single instruction, while throughput isdefined as the number of instructions processed per second

Question No : 42 of 52 Marks: 2 (Budgeted Time 4 Min)

Which attributes a device should have in order to be qualified as a master device?

Answer (Please click here to Add Answer)

A Master must have the capability to place addresses on the address bus and direct the bus activity during a buscycle

For More Visit VU Answer

Question No : 43 of 52 Marks: 2 (Budgeted Time 4 Min)

Differentiate between Spatial Locality and Temporal Correlation.

Answer (Please click here to Add Answer)

Spatial Locality This would mean that in a part of a program, if we have a particular address being accessed then it is highly probable that the data available at the next address would be highly accessed.

Temporal Correlation In this case, we say that at a particular time, if we have utilized a particular part of the memory then we might access the adjacent parts very soon.

Question No : 44 of 52 Marks: 2 (Budgeted Time 4 Min)

Name any two methods that are used to measure I/O subsystem performance.

Answer (Please click here to Add Answer)

Question No : 45 of 52 Marks: 3 (Budgeted Time 6 Min)

Differentiate between sender overhead and receiver overhead related to performance issues of networks.

Answer (Please click here to Add Answer)

Sender overhead It is the time for the processor to inject message in to the network.

Receiver overhead It is the time for the processor to pull the message from the network.

Question No : 46 of 52 **Marks: 3 (Budgeted Time 6 Min)**

Write down the categories of instructions supported by FALCON-A processor and also state that in type 1 instruction format of FALCON-A, how many bits are reserved for the op-code?

Answer (Please click here to Add Answer)

Question No : 47 of 52 **Marks: 3 (Budgeted Time 6 Min)**

Find the average rotational latency (in milliseconds) of the disk if it rotates at 15,000 rpm.

Answer (Please click here to Add Answer)

Question No : 48 of 52 **Marks: 3 (Budgeted Time 6 Min)**

If a DRAM has 512 rows and its refresh time is 8ms, what should be the average frequency of row refresh operation?

Answer (Please click here to Add Answer)

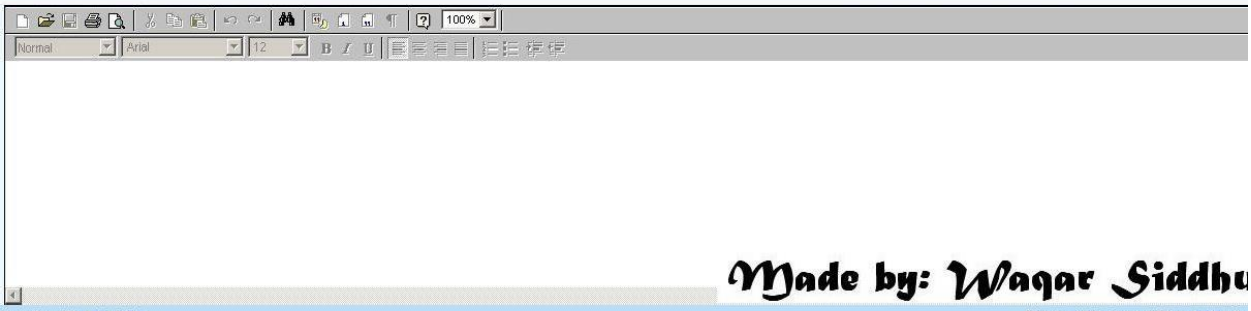
Refresh time =8ms
Number of rows =512
Therefore we have to do 512 row refresh operations in a 9 ms interval, in other words
one row refresh operation every = ($8*10^{-3}$)/512
=$1.56 * 10^{-5}$ second

Question No : 49 of 52 Marks: 5 (Budgeted Time 10 Min)

Briefly explain the following features of FALCON-E.

a. Number of registers
b. Size of each register
c. Memory word size
d. Memory space

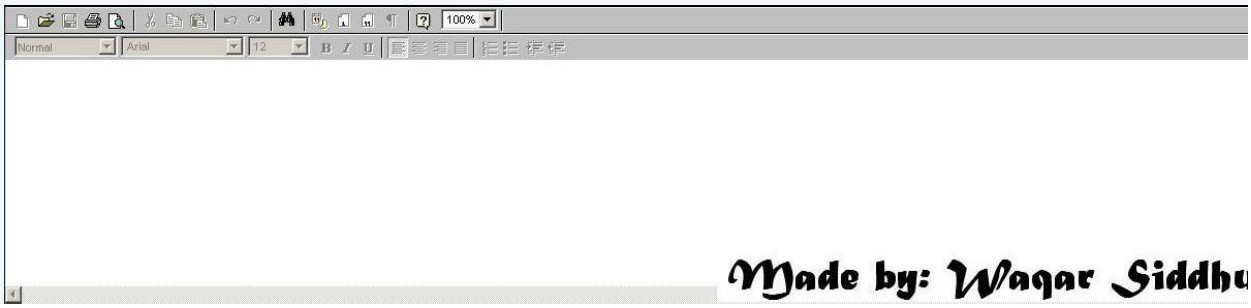
Answer (Please click here to Add Answer)



Question No : 50 of 52 Marks: 5 (Budgeted Time 10 Min)

Explain briefly how the interrupting module is identified in software polling and also point out the major drawback of Software Poll and Daisy Chain.

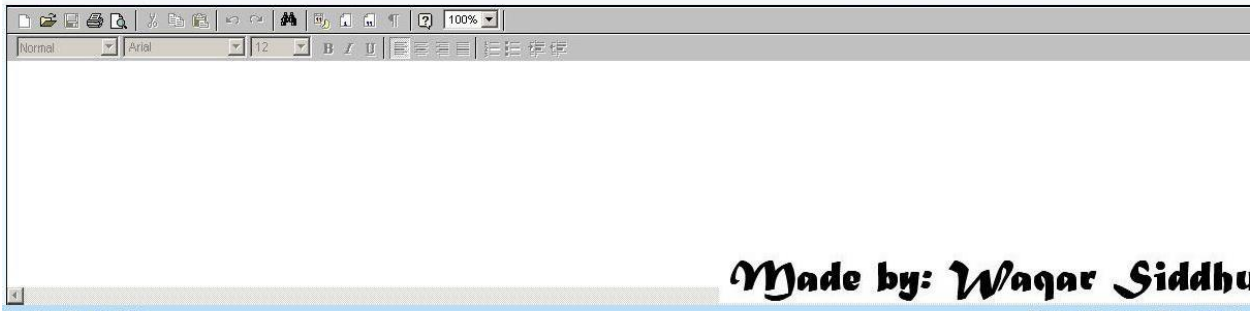
Answer (Please click here to Add Answer)



Question No : 51 of 52 Marks: 5 (Budgeted Time 10 Min)

According to the Radix conversion algorithm, convert the hexadecimal number $C4_{16}$ to base 10 (Write down all the steps which are involved in conversion).

Answer (Please click here to Add Answer)



Question No : 52 of 52 Marks: 5 (Budgeted Time 10 Min)

Find the average access time of a level of memory hierarchy if the hit rate is 80%. The memory access takes 10ns on a hit and 100ns on a miss.

Answer (Please click here to Add Answer)