CS501 Final Term Papers By Waqar (File 1)

Question No : 1 of 52 Marks: 1 (Budgeted Time 1 Min)

What does the instruction "ldr R3, 58" of SRC do?

Answer (Please select your correct option) VuAnswers.com

- it will load the register R3 with the contents of the memory location M [PC+58] correct
- It will load the register R3 with the relative address itself (PC+58).
- It will store the register R3 contents to the memory location M [PC+58]
- No operation

Question No : 2 of 52 Marks: 1 (Budgeted Time 1 Min)

What functionality is performed by the instruction "lar R3, 36" of SRC?

Answer (Please select your correct option) VuAnswers.com

- it will load the register R3 with the contents of the memory location M [PC+36]
- It will load the register R3 with the relative address itself (PC+36). correct
- It will store the register R3 contents to the memory location M [PC+36]
- No operation

Question No : 3 of 52 Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the SRC processor?

Answer (Please select your correct option) VuAnswers.com

- 8 bits
- 16 bits
- 32 bits correct
- 64 bits

Question No : 4 of 52 Marks: 1 (Budgeted Time 1 Min)

What does the word 'D' in the 'D-flip-Flop' stands for?

Answer (Please select your correct option)

- Data **correct**
- Digital
- Dynamic
- Double

Question No : 5 of 52 Marks: 1 (Budgeted Time 1 Min)

Almost every commercial computer has its own particular ---------- language

Answer (Please select your correct option)

- assembly language **correct**
- English language
- Higher level language
- 3GL

Question No : 6 of 52 Marks: 1 (Budgeted Time 1 Min)

Which field of the machine language instruction is the "**type of operation**" that is to be performed?

Answer (Please select your correct option)

- Op-code (or the operation code) **correct**
- CPU registers
- Memory cells
- I/O locations

For More Visit VU Answer

Question No : 7 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is/are defined as the time required processing a single instruction.

Answer (Please select your correct option)

- Latency and Throughput
- Latency correct
- Throughput
- Hazards

Question No : 8 of 52 Marks: 1 (Budgeted Time 1 Min)

In pipelining ---------- is increased by overlapping the instruction execution

Answer (Please select your correct option)

- Latency
- Throughput correct
- Execution time
- Clock speed

Question No : 9 of 52 Marks: 1 (Budgeted Time 1 Min)

Which of the following register(s) takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system?

Answer (Please select your correct option)

- Instruction Register
- Memory address register correct
- Memory Buffer Register
- Registers A and C

Question No : 10 of 52 Marks: 1 (Budgeted Time 1 Min)

In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

Answer (Please select your correct option)

- Direct Addressing Mode — correct
- Immediate addressing mode
- Indirect Addressing Mode
- Register (Direct) Addressing Mode

Question No : 11 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following type of error occurs when a 0 is received instead of a stop bit (which is always a 1)?

Answer (Please select your correct option)

- Framing error — correct
- Parity error
- Over-run error
- Under-run error

Question No : 12 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

Answer (Please select your correct option)

- Partial decoding — correct
- Full encoding
- Partial multiplexing
- Half encoding

Question No : 13 of 52 Marks: 1 (Budgeted Time 1 Min)

Consider Falcon A, with 16 address lines, the total address space is _____ Kbytes.

Answer (Please select your correct option)

- 2 ^ 16 correct
- 2 ^ 10
- 2 ^ 6
- 2 ^ 8

Question No : 14 of 52 Marks: 1 (Budgeted Time 1 Min)

CPU can exchange data with a peripheral device using _____ technique.

Answer (Please select your correct option)

- Memory Contention
- Direct Memory Access correct
- Pre-fetching
- Pipelining

Question No : 15 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one of the following is **NOT** a technique used when the CPU wants to exchange data with peripheral device?

Answer (Please select your correct option)

- Direct Memory Access
- Interrupt driven I/O
- Programmed I/O
- Virtual Memory correct

For More Visit VU Answer

Question No : 16 of 52 Marks: 1 (Budgeted Time 1 Min)

Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

Answer (Please select your correct option)

- IRET correct
- IRQ
- INT
- NMI

Question No : 17 of 52 Marks: 1 (Budgeted Time 1 Min)

---------- is the time needed by the CPU to recognize (not service) an interrupt request.

Answer (Please select your correct option)

- Interrupt Latency correct
- Response Deadline
- Timer delay
- Throughput

Question No : 18 of 52 Marks: 1 (Budgeted Time 1 Min)

In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

- External and Internal
- CPU and I/O correct
- CPU and Memory
- Memory and I/O

Question No : 19 of 52 Marks: 1 (Budgeted Time 1 Min)

In FALCON-A assembler and simulator (FALSIM), variables are defined by using the _____ directive.

Answer (Please select your correct option)

- .bin
- .equ — correct
- .iret
- .end

Question No : 20 of 52 Marks: 1 (Budgeted Time 1 Min)

In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

Answer (Please select your correct option)

- DMA memory unit
- DMA controller — correct
- Control software
- Programmed I/O

Question No : 21 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

Answer (Please select your correct option)

- Programmed I/O
- Interrupt driven I/O
- Direct memory access — correct
- Polling

Question No : 22 of 52 Marks: 1 (Budgeted Time 1 Min)

A component connected to the system bus and having control of it during a particular bus cycle is called _____.

Answer (Please select your correct option)

- Address decoder
- BIOS
- Master component — correct
- Slave component

Question No : 23 of 52 Marks: 1 (Budgeted Time 1 Min)

A Hard Disk sector has the _____ parts.

Answer (Please select your correct option)

- Header only
- Data section and a trailer
- Data section only
- Header, data section and a trailer — correct

Question No : 24 of 52 Marks: 1 (Budgeted Time 1 Min)

CRC has _____overhead as compared to Hamming code.

Answer (Please select your correct option)

- Equal
- Greater
- Lesser — correct
- Absolutely no

For More Visit VU Answer

Question No : 25 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ are computed by the ALU and stored in processor status register.

Answer (Please select your correct option)

- Condition Codes — correct
- Control Signals
- Flip Flops
- Multiplexers

Question No : 26 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ occurs when the exponent is too large and can not be represented in the exponent field.

Answer (Please select your correct option)

- Underflow
- Overflow — correct
- Rounding Off
- Normalization

Question No : 27 of 52 Marks: 1 (Budgeted Time 1 Min)

In Single-Precision Binary Floating Point Representation the size of exponent is _____.

Answer (Please select your correct option)

- 8-bits — correct
- 11-bits
- 1-bits
- 23-bits

For More Visit VU Answer

Question No : 28 of 52 Marks: 1 (Budgeted Time 1 Min)

The _____ is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus.

Answer (Please select your correct option)

- Memory address register (MAR) correct
- Program counter register
- Accumulator register
- Instruction register

Question No : 29 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is a place for safe storage and provides the fastest possible storage after the registers.

Answer (Please select your correct option)

- Hard Disk
- Cache correct
- Compact Disk
- Floppy Disk

Question No : 30 of 52 Marks: 1 (Budgeted Time 1 Min)

For a request for data, if the data is available in the cache it results in a _____.

Answer (Please select your correct option)

- Cache Miss
- Spatial Locality
- Temporal Locality
- Cache Hit correct

Question No : 31 of 52 Marks: 1 (Budgeted Time 1 Min)

For write to complete in Write through, the CPU has to wait. This wait state is called _____.

Answer (Please select your correct option)

- Write Through
- Write Back
- Write Allocate
- Write Stall

correct

Question No : 32 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ contains permanent pattern of data that cannot be changed.

Answer (Please select your correct option)

- RAM
- Hard Disk
- Cache
- ROM

correct

Question No : 33 of 52 Marks: 1 (Budgeted Time 1 Min)

In Control Field of page table, _____ indicate the availability of page in main memory.

Answer (Please select your correct option)

- Access Control Bits
- Used Bits
- Presence Bits

correct

- Redundant Bits

For More Visit VU Answer

Question No : 34 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____technique memory is divided into segments of variable sizes depending upon the requirements.

Answer (Please select your correct option)

- Multiplexing
- Segmentation — correct
- Hamming code
- Partial decoding

Question No : 35 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ depends upon the average number of calls and the service time taken by a particular server.

Answer (Please select your correct option)

- Throughput — correct
- Latency
- Poisson Distribution
- Response Time

Question No : 36 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is also called traffic intensity and its value must be between 0 and 1.

Answer (Please select your correct option)

- Little's Law
- Poisson Distribution
- Server Utilization — correct
- SPEC

For More Visit VU Answer

Question No : 37 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is the maximum rate at which data can be transmitted through networks.

Answer (Please select your correct option)

- Transmission Time
- Latency
- Transport Latency
- Bandwidth

correct

Question No : 38 of 52 Marks: 1 (Budgeted Time 1 Min)

The time for the message to pass through the network, except the time of flight is called _____.

Answer (Please select your correct option)

- Transmission Time

correct

- Latency
- Transport Latency
- Bandwidth

Question No : 39 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ refers to the interconnection of machines in a building or a campus.

Answer (Please select your correct option)

- SAN
- LAN

correct

- WAN
- MAN

Question No : 40 of 52 Marks: 1 (Budgeted Time 1 Min)

SPARC (Scalable Processor Architecture) is an example of _____architecture.

Answer (Please select your correct option)

- CISC
- RISC

correct

- SRC
- FALCON

Question No : 41 of 52 Marks: 2 (Budgeted Time 4 Min)

What is distributed computing?

Answer (Please click here to Add Answer)

In distributed computing, all elements which are interconnected operate under oneoperating system. To a user, it appears as a virtual uni-processor system.

Question No : 42 of 52 Marks: 2 (Budgeted Time 4 Min)

Write any two differences between EAGLE and Modified EAGLE.

Answer (Please click here to Add Answer)

The modified EAGLE is an improved version of the processor EAGLE. there were several limitations in EAGLE, and these have been remedied in the modified EAGLE processor.

Question No : 43 of 52 Marks: 2 (Budgeted Time 4 Min)

Differentiate between selector channel and multiplexer channel.

Answer (Please click here to Add Answer)

Selector Channel It is the DMA controller that can do block transfers for several devices but only one at a time.
Multiplexer Channel It is the DMA controller that can do block transfers for several devices at once.

Question No : 44 of 52 Marks: 2 (Budgeted Time 4 Min)

Differentiate between PROM and EPROM.

Answer (Please click here to Add Answer)

PROM The PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into onlyonce. For PROM, the writing process is performed electrically in the field. PROMs provide flexibility andconvenience.

EPROM Erasable Programmable Read-only Memory or EPROM chips have quartz windows and by applying ultravioletlight erase the data can be erased from the EPROM. Data can be restored in an EPROM after erasure. EPROMsare more expensive than PROMs and are generally used for prototyping or small-quantity, special purposework.

Question No : 45 of 52 Marks: 3 (Budgeted Time 6 Min)

How can you define an instruction set? Name the essential elements of computer instructions.

Answer (Please click here to Add Answer)

INSTRUCTION SET An instruction set is a collection of all possible machine language commands that areunderstood and can be executed by a processor.
ESSENTIAL ELEMENTS OF COMPUTER INSTRUCTIONS:There are four essential elements of an instruction; **the type of operation to be performed**,**the place to find the source operand(s)**, the **place to store the result(s)** and the **source of the next instruction** to be executed by the processor.

Question No : 46 of 52 Marks: 3 (Budgeted Time 6 Min)

What is the relationship between hard disk Platters, Tracks and Sectors?

Answer (Please click here to Add Answer)

A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is dividedinto tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, beforethe actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header thereis a trailer. Every sector has three parts: a header, data section and a trailer.

Question No : 47 of 52 Marks: 3 (Budgeted Time 6 Min)

Find out the Sign, Significand and Exponent from the following floating point number.

-0.7×10^{-4}

Answer (Please click here to Add Answer)

Sign = 0
Significand= 0.7
Exponent= -4
Base = 10= fixed for given type of representation

Question No : 48 of 52 Marks: 3 (Budgeted Time 6 Min)

What is the use of translation lookaside buffer (TLB) and how it is implemented inside the CPU?

Answer (Please click here to Add Answer)

To speed up the process of virtual address translation, translation Lookaside buffer (TLB) is implemented as a small cache inside the CPU, which stores the most recent page table entry referencemade in the MMU.

Question No : 49 of 52 Marks: 5 (Budgeted Time 10 Min)

Write the Structural RTL description for "un-conditional jump" instruction i.e. **jump [ra+c2].**

Answer (Please click here to Add Answer)

Step	RTL
T0-T2	Instruction Fetch
T3	(ra=0): A← PC, (ra≠0): A ← R[ra];
T4	C ← A + c2(sign extend);
T5	PC ← C;

Step	RTL
T0-T2	Instruction fetch
T3	n<4..0> ← IR<4..0>;
T4	C ← (Nα0) © R[rb]<15..N>;
T5	R[ra] ← C;

Question No : 50 of 52 Marks: 5 (Budgeted Time 10 Min)

A hard disk with 10 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?

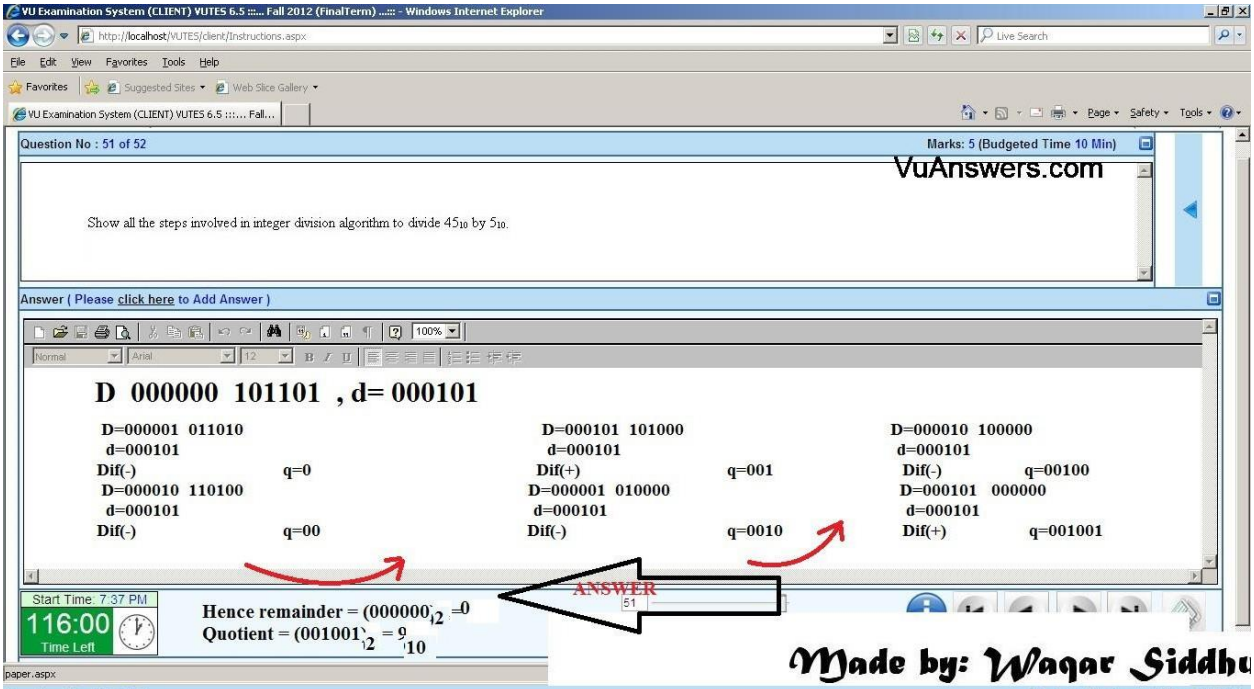
Answer (Please click here to Add Answer)

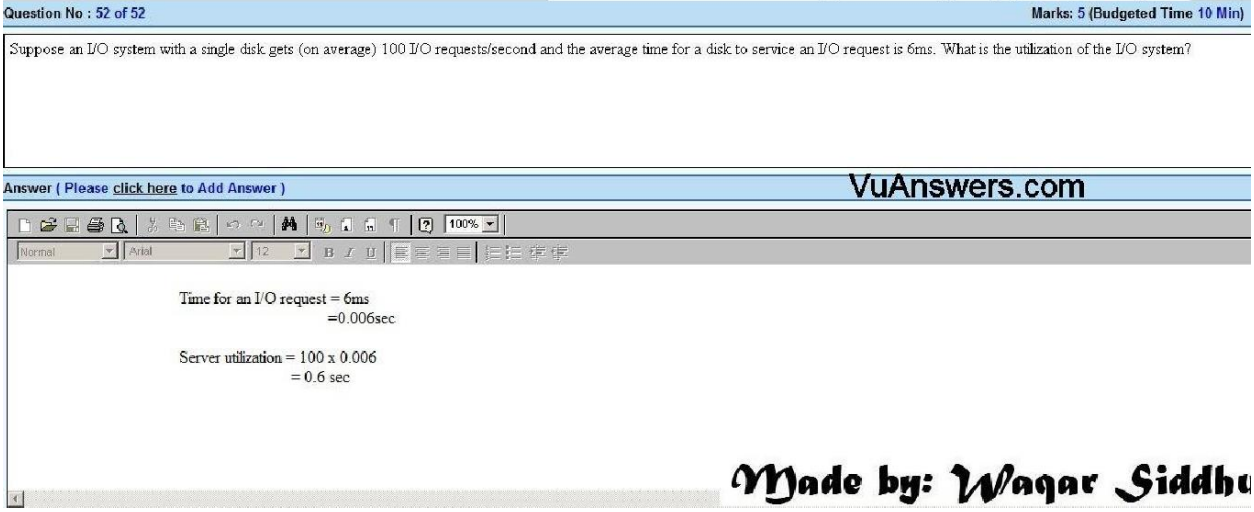
512 bytes x 512

sectors=0.2MB/track

0.2MB x 1024 tracks =0.2GB/platter

Therefore the hard disk has the total capacity of 10 x 0.2=2GB


VU Examination System (CLIENT) VUTES 6.5 ::::.. Fall 2012 (FinalTerm) ..::: - Windows Internet Explorer
Question No : 51 of 52
Marks: 5 (Budgeted Time 10 Min)
VuAnswers.com
Show all the steps involved in integer division algorithm to divide 45₁₀ by 5₁₀.
Answer (Please click here to Add Answer)
D 000000 101101 , d= 000101
D=000001 011010
d=000101
Dif(-) q=0
D=000010 110100
d=000101
Dif(-) q=00
D=000101 101000
d=000101
Dif(+) q=001
D=000001 010000
d=000101
Dif(-) q=0010
D=000010 100000
d=000101
Dif(-) q=00100
D=000101 000000
d=000101
Dif(+) q=001001
ANSWER
Start Time: 7:37 PM
116:00
Time Left
Hence remainder = (000000)₂ =0
Quotient = (001001)₂ = 9₁₀
Made by: Waqar Siddhu


Question No : 52 of 52
Marks: 5 (Budgeted Time 10 Min)
Suppose an I/O system with a single disk gets (on average) 100 I/O requests/second and the average time for a disk to service an I/O request is 6ms. What is the utilization of the I/O system?
Answer (Please click here to Add Answer)
VuAnswers.com
Time for an I/O request = 6ms
=0.006sec
Server utilization = 100 x 0.006
= 0.6 sec
Made by: Waqar Siddhu