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CS302 Past Papers

(Paper 1)

Question No : 1 of 52	Marks: 1 (Budgeted Ti	ime 1 Min) 🗏
The diagram given below represents		_
A		
B		
		•
Answer (Please select your correct option)	VuAnswers.com	
C Demorgans law		
Associative law		
Product of sum form		
Sum of product form COFFOCT	Made by: Wagar S	iddhu
Question No : 2 of 52	Marks: 1 (Budgeted Ti	ime 1 Min)
The decimal *8" is represented asusing Gray-Code.		A
Answer (Please select your correct option)	VuAnswers.com	<u> </u>
0011	V dAnswers.com	
c		
1100		
correct		
1000		
c		
1010		
C	Made by: Wagar S	iddhu
Occupation No. 2 of 52	Marks: 1 (Budgeted Ti	
Question No : 3 of 52	marks: 1 (Buagetea 11	ime 1 Min)
The binary numbers $A = 1100$ and $B = 1001$ are applied to the inputs of a comparator. What are the output levels?		
Answer (Please select your correct option)	VuAnswers.com	<u></u>
A > B = 1, A < B = 0, A < B = 1	, 41115, 615, 6611	
C		
A > B = 0, A < B = 1, A = B = 0		
0		
A > B = 1, A < B = 0, A = B = 0		
A > B = 0, A < B = 1, A = B = 1	Made but \$40	12.4.4.L.
	Made by: Wagar S	/144D

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Question No : 4 of 52	Marks: 1 (Budgeted Time 1 Min)
The simplest of the Encoders are theEncoders	
Answer (Please select your correct option)	VuAnswers.com
C 2*1-to-n	
n-to-2n	
C 2~to-n	St
n-to-2+1	Made by: Waqar Siddh
Question No : 5 of 52	Marks: 1 (Budgeted Time 1 Min)
Using multiplexer as parallel to serial converter requires connected to the	- Nonepieces
Answer (Please select your correct option)	VuAnswers.com
A parallel to serial converter circuit	
	correct
A counter circuit	
A BCD to Decimal decoder	
A 2-to-8 bit decoder	Made by: Wagar Siddh
Question No : 6 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	
Answer (Please select your correct option)	VuAnswers.com
ENP, ENT	'' V = V V V ===
correct	
ENI, ENC	
ENP, ENC	
ENT, ENI	244 1 1 2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
	Made by: Magar Siddh

	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
inswer (Please select your correct option)	VuAnswers.com
	V UATISWELS,COM
The next state of a given present state	
The previous state of a given present state	
Both the next and previous states of a given state	
	correct
The state diagram shows only the inputs/outputs of a given states	
Question No : 8 of 52	Marks: 1 (Budgeted Time 1 Min)
nswer (Please select your correct option)	VuAnswers.com
1	
0	
2	
c 3	
4	correct Made by: Waqar Siddh
hestion No : 9 of 52	
395 400	
$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of	Marks: 1 (Budgeted Time 1 Min)
$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of	
nswer (Please select your correct option) $C \begin{tabular}{l} \label{eq:constraints} \hline (A+B)(A+\overline{B}+C)(\overline{A}+C) & \text{is an example of } \\ \hline \end{tabular}$	Marks: 1 (Budgeted Time 1 Min)
$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of	Vuanswers.com
nswer (Please select your correct option) C Sum of product form	VuAnswers.com

Question No : 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	
Answer (Please select your correct option)	VuAnswers.com
C Convert binary numbers to decimal	, G1115 11 OL D, GG111
Convert decimal numbers to binary	
Represent signed numbers	correct
Represent positive numbers	Made by: Waqar Siddh
Question No : 11 of 52	Marks: 1 (Budgeted Time 1 Min)
1011 – 101 =	
Note: both values are in binary	
Answer (Please select your correct option)	VuAnswers.com
c 1100	
C 0110	correct
0011	
c 1001	Made by: Wagar Siddh
Question No : 12 of 52	Marks: 1 (Budgeted Time 1 Min)
At $J=1$, and $K=1$, output of JK Flip-flop will be	
Answer (Please select your correct option)	VuAnswers.com
C Set	
Reset	
Toggle	correct
Invalid	
C	Made by: Magar Siddh

Question No : 10 of 52		Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to		
inswer (Please select your correct option)		VuAnswers.com
Convert binary numbers to decimal		VUAIISWELS,COIII
C Convert binary numbers to decimal		
Convert decimal numbers to binary		
Represent signed numbers		4
	correct	
Represent positive numbers		Made by: Wagar Siddl
Juestion No : 14 of 52		Marks: 1 (Budgeted Time 1 Min)
Using 15 digits (including the sign digit) notation the largest number that can be rep	resented is	
		172
nswer (Please select your correct option)		VuAnswers.com
999,999,999,999 × 10100		
0.999,999,999 × 10100		
999,999,999,999 × 1099		
0.999,999,999 × 10∞	correct	Made by: Waqar Siddh
luestion No : 15 of 52		Marks: 1 (Budgeted Time 1 Min)
The output of first 74HC163 counter is connected to and	_inputs of other 74HC1	
nswer (Please select your correct option)		VuAnswers.com
RCO, ENT, ENP	rect	
ENT, RCO, ENP		
ENP, RCO, ENT		
RCO, ENI, ENC		
		Made bu: 11/agar Siddl

Question No : 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	
Answer (Please select your correct option)	VuAnswers.com
C Convert binary numbers to decimal	
Convert decimal numbers to binary	
Represent signed numbers COPTS	ct
C Represent positive numbers	Made by: Waqar Siddh
Question No : 17 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
Maximizes the number of state variables that don't change in a group of related states	correct
Minimizes the number of state variables that don't change in a group of related states	
Minimizes the equivalent states	
Maximizes the equivalent states	Made by: Wagar Siddh
Question No : 18 of 52	Marks: 1 (Budgeted Time 1 Min)
In, the \overline{Q} output of the last flip-flop of the shift register is connected to the data input of the first flip	-flop.
Answer (Please select your correct option)	VuAnswers.com
C Moore machine	
Mealy machine	
Johnson counter COFFECT	
Ring counter	Made bu: 14/2001 Siddhi

Question No: 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	
Answer (Please select your correct option)	VuAnswers.com
C Convert binary numbers to decimal	V C
C Convert decimal numbers to binary	
Represent signed numbers	ect
Represent positive numbers	Made by: Wagar Siddh
Question No : 20 of 52	Marks: 1 (Budgeted Time 1 Min)
Flip flops are also called	
Answer (Please select your correct option)	VuAnswers.com
Bi-stable dualvibrators	
Bi-stable transformer	
Bi-stable multivibrators COPPO	et
Bi-stable singlevibrators	Made by: Waqar Siddh
Question No : 21 of 52	Marks: 1 (Budgeted Time 1 Min)
If S=1 and R=0, then Q(t+1) = for positive edge triggered flip-flop	
Answer (Please select your correct option)	VuAnswers.com
correct	
c I	
Invalid	
Input is invalid	Made bu: 14/agar Siddh

Question No : 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	2
Answer (Please select your correct option)	VuAnswers.com
Convert binary numbers to decimal	
Convert decimal numbers to binary	
Represent signed numbers	rrect
Represent positive numbers	Made by: Waqar Siddh
Question No: 23 of 52	Marks: 1 (Budgeted Time 1 Min)
Flip-flops are obsolete now.	
Answer (Please select your correct option)	VuAnswers.com
Edge-triggered	
Master-Slave COTTOCT T-Flip-flop	
D-Flip-flop	
	Made by: Waqar Siddhi
Question No : 24 of 52	Marks: 1 (Budgeted Time 1 Min)
Bi-stable devices remain in either of their states unless the inputs force the device to switch	its state.
Answer (Please select your correct option)	VuAnswers.com
C Ten	
C Eight	
Three	
Two COFFEC	Made by: Magar Siddh

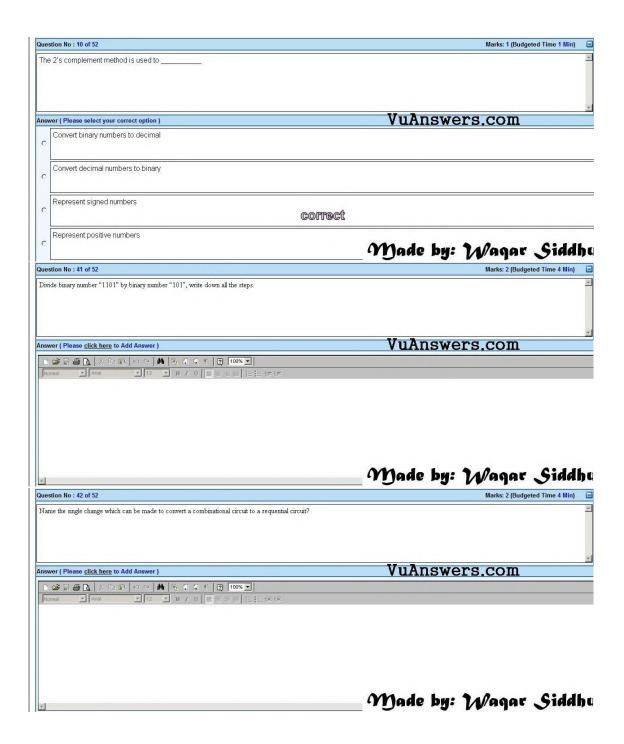
Question No : 10 of 52		Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	-1	
nswer (Please select your correct option)		VuAnswers.com
Convert binary numbers to decimal		
Convert decimal numbers to binary		
Represent signed numbers	com	ect
Represent positive numbers		Made by: Waqar Siddh
Question No : 26 of 52		Marks: 1 (Budgeted Time 1 Min)
RCO Stands for		
Answer (Please select your correct option)		VuAnswers.com
Reconfiguration Counter Output		
Reconfiguration Clock Output		
Ripple Counter Output		
Ripple Clock Output	correct	Made by: Waqar Siddh
Question No : 27 of 52		Marks: 1 (Budgeted Time 1 Min)
The Sequential circuit, whose output is determined by the c	urrent state only is known as	
Answer (Please select your correct option)		VuAnswers.com
Moore Machine	correct	
Mealy Machine		
Counter		
Flip Flop		Made hu: 14/200 Siddh

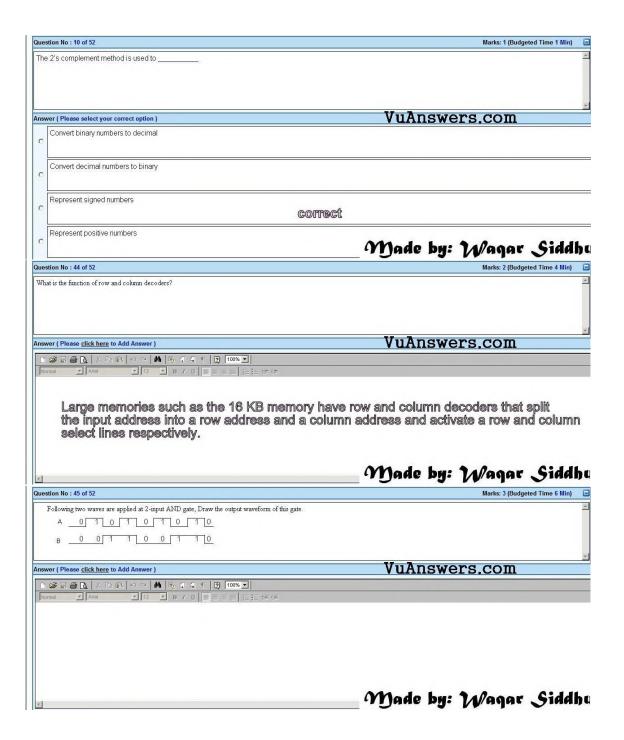
Question No : 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	
Answer (Please select your correct option)	VuAnswers.com
Convert binary numbers to decimal	<u> </u>
Convert decimal numbers to binary	
Represent signed numbers	correct
C Represent positive numbers	Made by: Magar Siddh
Question No : 29 of 52	Marks: 1 (Budgeted Time 1 Min)
The output of this circuit is always +Vec A	
Answer (Please select your correct option)	VuAnswers.com
c 0 0	
C COFFE	ect
c A	Made by: Wagar Siddh
Question No : 30 of 52	Marks: 1 (Budgeted Time 1 Min)
Which is not characteristic of a shift register?	
Answer (Please select your correct option)	VuAnswers.com
Serial in/parallel in	Tect
Serial in/parallel out	
Parallel in/serial out	
Parallel in/parallel out	Made by: Wagar Siddh

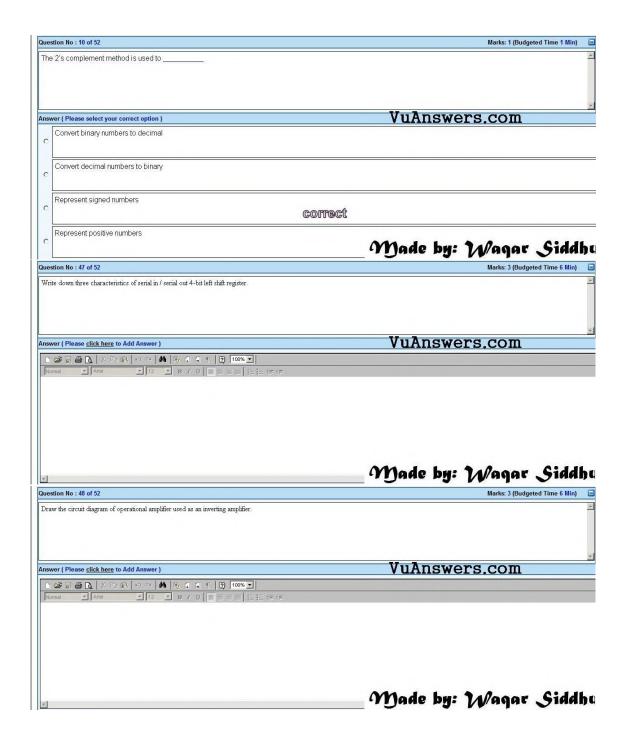
Question No : 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	
Answer (Please select your correct option)	VuAnswers.com
Convert binary numbers to decimal	, G1115 11 OL D, GG111
Convert decimal numbers to binary	
Represent signed numbers	prect
Represent positive numbers	Made by: Waqar Siddh
Question No : 32 of 52	Marks: 1 (Budgeted Time 1 Min)
Smallest unit of binary data is a	
Answer (Please select your correct option)	VuAnswers.com
C Bit CONTROL	
C Nibble	
C Byte	
C Word	Made by: Wagar Siddh
Question No : 33 of 52	Marks: 1 (Budgeted Time 1 Min)
The of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines	
Answer (Please select your correct option)	VuAnswers.com
C Write Time	
Refresh Time	
C Refresh Time	
Access Time COPPOCT	Made by: Magar Siddho

Question No : 10 of 52	Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to	
Answer (Please select your correct option)	VuAnswers.com
Convert binary numbers to decimal	
Convert decimal numbers to binary	
Represent signed numbers	correct
Represent positive numbers	Made by: Waqar Siddh
Question No : 35 of 52	Marks: 1 (Budgeted Time 1 Min)
Inswer (Please select your correct option)	VuAnswers.com
First In, First Out	A Comment of the Comm
Fly in, Fly Out	
Fast in, Fast Out	
None of given options	Made by: Wagar Siddh
Question No : 36 of 52	Marks: 1 (Budgeted Time 1 Min)
If the FIFO Memory output is already filled with data then	
Answer (Please select your correct option)	VuAnswers.com
It is locked; no data is allowed to enter	† WILLDWOLD,COM
It is not locked, the new data overwrites the previous data.	
Previous data is swapped out of memory and new data enters	correct
None of given options	Made by: 14/200 Siddh

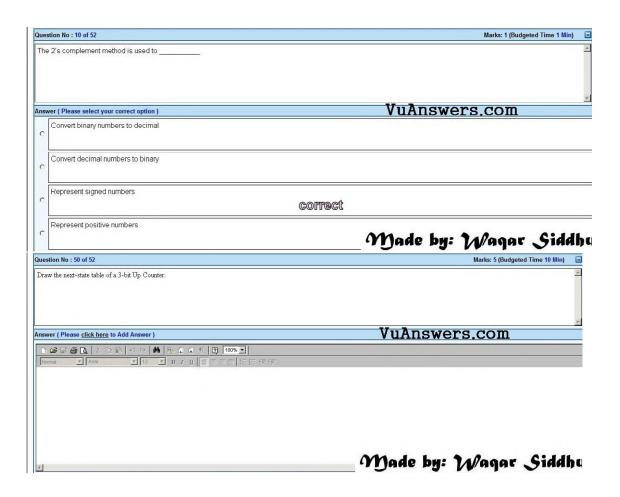
Question No : 10 of 52		Marks: 1 (Budgeted Time 1 Min)
The 2's complement method is used to		
Answer (Please select your correct option)		VuAnswers.com
C Convert binary numbers to decimal		<u> </u>
Convert decimal numbers to binary		
Represent signed numbers	cor	rect
Represent positive numbers		Made by: Wagar Siddh
Question No : 38 of 52		Marks: 1 (Budgeted Time 1 Min)
A flash A/D converter uses :		
Answer (Please select your correct option)		VuAnswers.com
Counters		
c	correct	not sure
Flip-flops		
C Op-amps		
C An integrator		Made by: Waqar Siddh
Question No : 39 of 52		Marks: 1 (Budgeted Time 1 Min)
LUT is an acronym for		
Answer (Please select your correct option)		VuAnswers.com
C Look Up Table	correct	
Local User Terminal		
Least Upper Time Period		
None of given options		Made by: Wagar Siddh

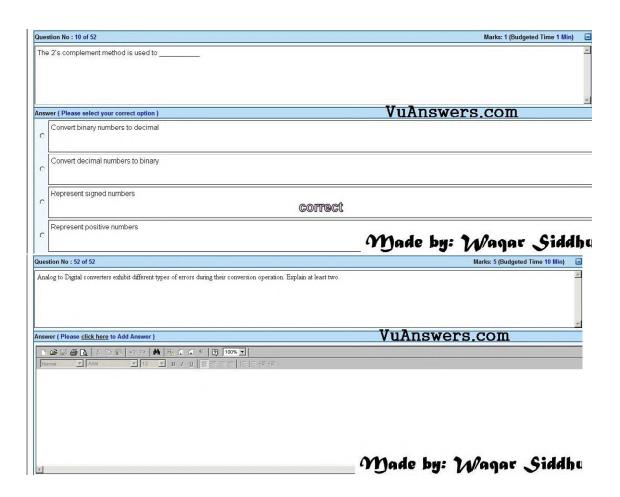




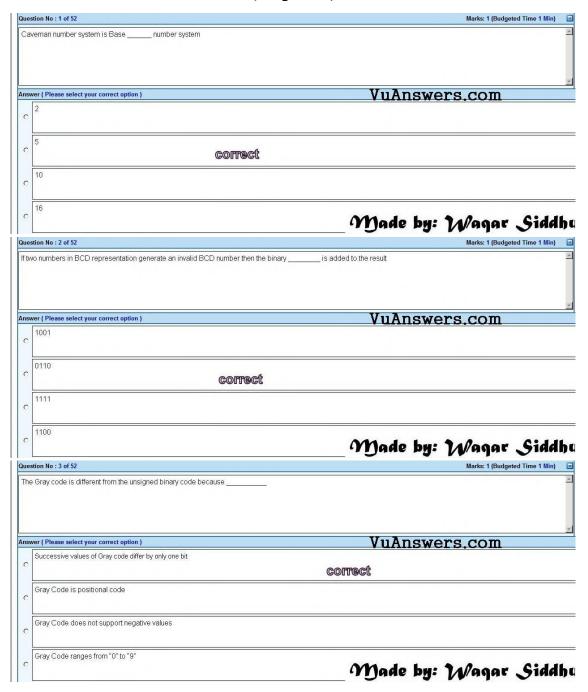


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(Paper 2)



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Question No : 4 of 52	Marks: 1 (Budgeted Time 1 Min)
'74ALS' stands for	
	V3
nswer (Please select your correct option)	VuAnswers.com
C Advanced Low-frequency Schottky TTL	
Advanced Low-dissipation Schottly TTL	
Advanced Low-Power Schottky TTL	
	correct
Advanced Low-propagation Schottky TTL	Made by: Waqar Siddh
Question No : 5 of 52	Marks: 1 (Budgeted Time 1 Min)
The 3-variable Karnaugh Map (K-Map) has cells for min or max terms	mains. I pudgeted time I minj
nswer (Please select your correct option)	VuAnswers.com
B COITES	ct
c 12	
c 18	Made by: Waqar Siddh
Question No : 6 of 52	Marks: 1 (Budgeted Time 1 Min)
The cell marked 6 in 4-variable K-Map represent minterm 6 or the maxterm 6 having the follow	ing binary value of variables A, B, C and D.
inswer (Please select your correct option)	VuAnswers.com
A=1, B=1, C=0, D=0	Y GIIID WOLD, COM
A=0, B=1, C=1, D=0 CONTROC A=0, B=0, C=1, D=1	t .
C	
C A=1, B=0, C=0, D=1	Made bu: Magar Siddh

Question No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min)
The PROM consists of a fixed non-programmable	Gate array configured as a decoder.			4
Answer (Please select your correct option)		VuAnswe	rs.com	
c AND	correct			
OR				
c NOT				
XOR		Made by:	Wagar	Siddh
Question No : 8 of 52			Marks: 1 (Budge	ted Time 1 Min)
In a sequential circuit the next state is determined by	and			×
Answer (Please select your correct option)		VuAnswe	rs.com	
State variable, current state C Current state, flip-flop output				
C Current state and external input	correct			
Input and clock signal applied		Made by:	Wagar	Siddh
Question No : 9 of 52			Marks: 1 (Budge	ted Time 1 Min)
In CMOS 5 Volt series, input voltage for Logic high signal (Vi	μ) is in the range ofvolts.			_
Answer (Please select your correct option)		VuAnswe	rs.com	
c 3.5 to 5	correct			
4.5 to 5				
0 to 5				
0 to 3.5		Made bu:	Magar	Siddh

		Marks: 1 (Budge	ted Time 1 Min) 🔲
Gate array configured as a decoder.			A
	ViiAngwe	rg com	_
	V GIIISWC	.r.b.com	
correct			
	Made bu:	Magar	Siddhu
			<u>^</u>
			₹
	VuAnswe	rs.com	
correct			
	Made bu:	Magar	Siddhu
nutative Law for Multiplication?			<u> </u>
anter passingui protest e comprise in artistoni. Il portuguizzanti cole			
			▼
	VuAnswe	rs.com	
correct			
	Made bu:	Magar	Siddhu
	COPPOCT	VuAnswe Correct VuAnswe Correct VuAnswe Correct VuAnswe Correct	VuAnswers.com Correct VuAnswers.com Correct VuAnswers.com Correct VuAnswers.com Marks: 1 (Budget Marks: 1 (Budget) VuAnswers.com

Question No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min) 🗏
The PROM consists of a fixed non-programmable	Gate array configured as a decoder.			^
Answer (Please select your correct option)		VuAnswe	ers com	
AND		+ QIIIID WC	JI D.OOM	
C	correct			
OR				
C				
NOT				
C				
XOR				
C		Made by:	Wagar	Siddh
Question No : 14 of 52			Marks: 1 (Budge	
The design and implementation of synchronous counters start from				_
Answer (Please select your correct option)		VuAnswe	ers.com	
Truth table				
K-map				
C				
State table				
C				
State diagram	11.00000000		2 12	
C	correct	Made by:	Magar	Siddh
Question No : 15 of 52			Marks: 1 (Budge	
In a state diagram, the transition from a current state to the next stat	e is determined by and			_
				*
Answer (Please select your correct option)		VuAnswe	ers.com	
Current state, inputs				
	correct			
Current state, outputs				
C				
Previous state, inputs				
C				
Previous state, outputs				
C		Made by:	Magar	Siddh

Question No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min) 🔳
The PROM consists of a fixed non-programmable	_ Gate array configured as a decoder.			A
Answer (Please select your correct option)		VuAnswe	rs com	_
c AND	correct	V UZIIID W C	LD.COM	
OR				
NOT				
CXOR		Made by:	Waqar	Siddhu
Question No : 17 of 52			Marks: 1 (Budge	ted Time 1 Min) 🔳
Answer (Please select your correct option) or n+2 (n plus 2)		VuAnswe	ers.com	×
2n (n multiplied by 2) 2n (2 raise to power n)	correct			
n² (n raise to power 2) Question No: 18 of 52		Made by:	Waqar Marks: 1 (Budge	
Flip flops are also called			mana. I jourge	<u></u>
Answer (Please select your correct option)		VuAnswe	rs.com	×
C Bi-stable dualvibrators				
Bi-stable transformer				
Bi-stable multivibrators	correct			
Bi-stable singlevibrators		Made by:	Wagar	Siddhu

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
The PROM consists of a fixed non-programmable Gate array configured as a definition of the programmable and the programmable grammable gram	pecoder.
nswer (Please select your correct option)	VuAnswers.com
and	
OR STREET	
NOT	
XOR	244 1 1 4 4 6 6 1 11
	Made by: Waqar Siddh
uestion No : 20 of 52	Marks: 1 (Budgeted Time 1 Min)
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop	
nswer (Please select your correct option)	VuAnswers.com
Doesn't have an invalid state	V driis wet s.com
COFFE	at the state of th
Sets to clear when both J = 0 and K = 0	
It does not show transition on change in pulse	
It does not accept asynchronous inputs	044 1 1 4 4 6 6 111
	Made by: Magar Siddh
uestion No : 21 of 52	Marks: 1 (Budgeted Time 1 Min)
The minimum time for which the input signal has to be maintained at the input of flip-flop is called of th	e flip-flop.
nswer (Please select your correct option)	VuAnswers.com
Set-up time	V diffiswers.com
C	
Pulse Stability time (PST)	
C	
Hold time	
correct	
Pulse Interval time	
C	Made bu: 11/agar Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
he PROM consists of a fixed non-programmable Gate a	rray configured as a decoder.
swer (Please select your correct option)	VuAnswers.com
AND	T dillion of b. oom
C	orrect
OR	
NOT	
XOR	244 1 1 4 4 4 2 2 2 2 2 2 2 2 2 2 2 2 2
	Made by: Magar Siddh
uestion No : 23 of 52	Marks: 1 (Budgeted Time 1 Min)
The divide-by-60 counter in digital clock is implemented by using two cascading cou	nters;
nswer (Please select your correct option)	VuAnswers.com
Mod-6, Mod-10	
© ©	orrect
Mod-50, Mod-10	
Mod-10, Mod-50	
1400-10, 1400-30	
The second of the	
Mod-50, Mod-6	MA 1-1 - A.A 0.110
	Made by: Waqar Siddh
uestion No : 24 of 52	Marks: 1 (Budgeted Time 1 Min)
The hours counter is implemented using	<u> </u>
	¥
nswer (Please select your correct option)	VuAnswers.com
Mod-10 and Mod-2 counters	
C	
A single decade counter and a flip-flop	
C A SALE COURT AND A MAP HOP	correct
0.1	
Only a single Mod-12 counter is required	
Mod-10 and Mod-6 counters	244 1 1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
	Made bu: Magar Siddhu

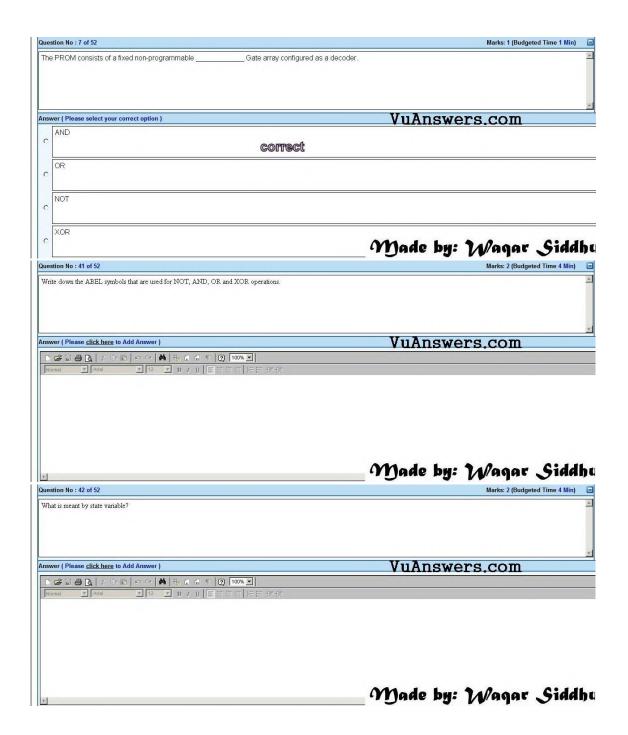
Question No : 7 of 52	Cata assessment		Marks: 1 (Budge	ted Time 1 Min)
The PROM consists of a fixed non-programmable	Gate array configured as a decoder.			
nswer (Please select your correct option)		VuAnswe	rs.com	
c AND	Comment and S			
	correct			
OR				
NOT				
XOR				especial de la company
C		Made by:	Wagar	Siddh
Question No : 26 of 52			Marks: 1 (Budge	
is used to simplify the circuit that determines the next state.				<u> </u>
nswer (Please select your correct option)		VuAnswe	rs.com	
State diagram				
Next state table				
C				
State reduction				
C				
State assignment				
C	correct	Made by:	Wagar	Siddh
Question No : 27 of 52			Marks: 1 (Budge	
The alternate solution for a demultiplexer-register combination circuit is				_
Inswer (Please select your correct option)		VuAnswe	rs.com	
Parallel in / Serial out shift register				
Serial in / Parallel out shift register	4			
	correct			
Parallel in / Parallel out shift register				
Serial in / Serial Out shift register				
C		Made bu:	Magar	Siddh

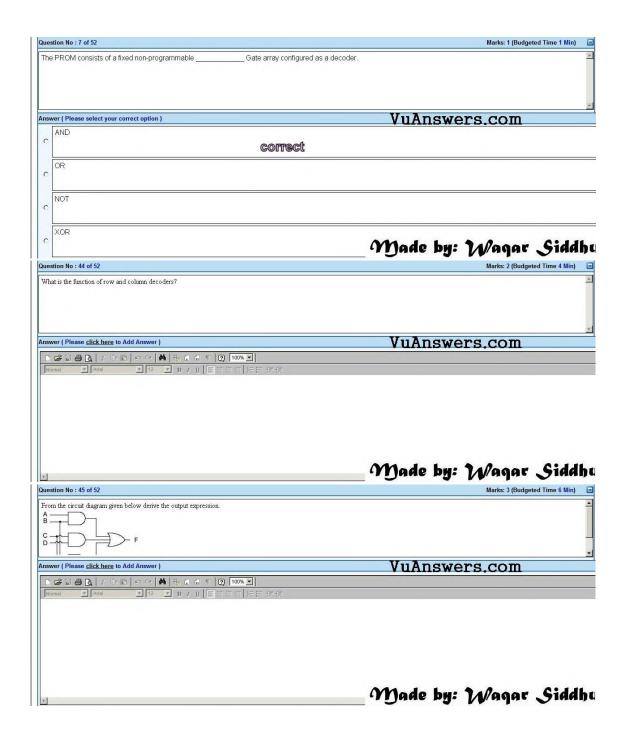
Question No: 7 of 52			Marks: 1 (Budge	ted Time 1 Min)
The PROM consists of a fixed non-programmable	Gate array configured as a decoder.			A
Answer (Please select your correct option)		VuAnswe	rs com	_
AND		* QZIIID W C	LD.COM	
C	correct			
OR				
NOT				
XOR		Made by:	Magar	Siddh
Question No : 29 of 52			Marks: 1 (Budge	
A GAL is essentially a				^
Answer (Please select your correct option)		VuAnswe	rs com	<u> </u>
Non-reprogrammable PAL		V GZIIIDWC	LD.COM	
PAL that is programmed only by the manufacturer				
Reprogrammable PAL	correct			
Reprogrammable PAL		Made by:	Magar	Siddh
Question No : 30 of 52		9.2.2.2	Marks: 1 (Budge	
Which is not characteristic of a shift register?				<u> </u>
Answer (Please select your correct option)		VuAnswe	rs.com	<u> </u>
Serial in/parallel in	correct			
Serial in/parallel out				
Parallel in/serial out				
Parallel in/parallel out		Made bu:	14/00er	Ciddh

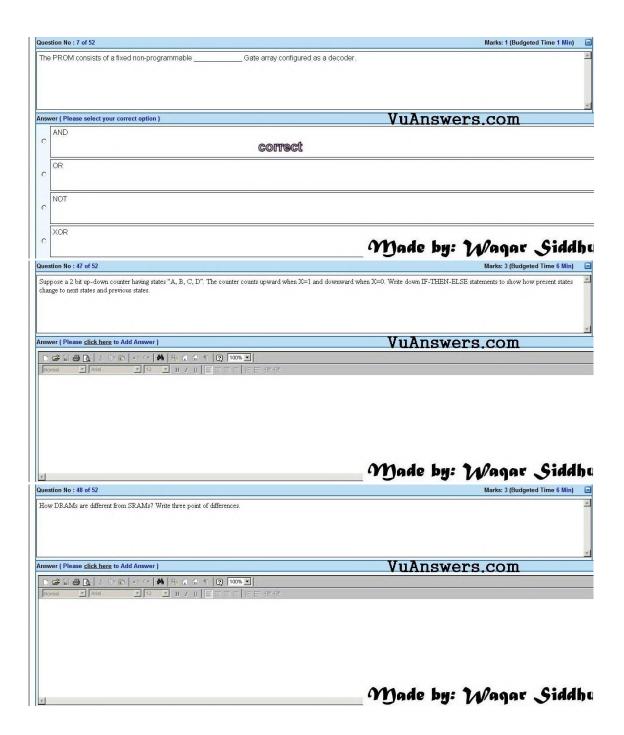
Question	1 No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min) 🔳
The Pf	ROM consists of a fixed non-programmable	Gate array configured as a decoder.			4
Answer	(Please select your correct option)		VuAnswe	rg com	
	ND		VULLISWE	L S.COIII	
c		correct			
c	3				
C	DT				
CX	DR		Made by:	Wagar	Siddhu
Question	1 No : 32 of 52			Marks: 1 (Budge	2000
A Nibb	le consists of bits				A.
Answer	(Please select your correct option)		VuAnswe	na aom	
2	(Frease select your confect option)		VUAIISWE	rs.com	
С					
c 4		correct			
С 8					
C 16			Made by:	Waqar	Siddhu
Question	n No : 33 of 52			Marks: 1 (Budge	ted Time 1 Min) 🔳
The ad-	tress, from which the data is read, is provided by				<u> </u>
Answer	(Please select your correct option)		VuAnswe	rs com	v
c De	pends on circuitry		V 411110 W C	10.0011	
C	one of given options				
C RA	AM				
С	icroprocessor	correct	Made by:	Magar	Siddhu

Question No : 7 of 52			Marks: 1 (Budge	eted Time 1 Min)
The PROM consists of a fixed non-programmable	Gate array configured as a decoder.			2
Answer (Please select your correct option)		VuAnswe	rs com	
AND				
C	correct			
OR				
NOT				
XOR		Made by:	Wagar	Siddh
Question No : 35 of 52			Marks: 1 (Budge	
Answer (Please select your correct option)		VuAnswe	rs.com	
Read Only Memory				
C First In First Out Memory	correct			
Flash Memory				
Fast Page Access Mode Memory		Made by:	Waqar	Siddh
Question No : 36 of 52			Marks: 1 (Budge	ted Time 1 Min)
If the FIFO Memory output is already filled with data then				*
Answer (Please select your correct option)		VuAnswe	rs.com	
It is locked; no data is allowed to enter				
It is not locked; the new data overwrites the previous dat	ta.			
Previous data is swapped out of memory and new data e	nters			
None of given options	COMPACT	Made bu:	14/00er	Ciddh

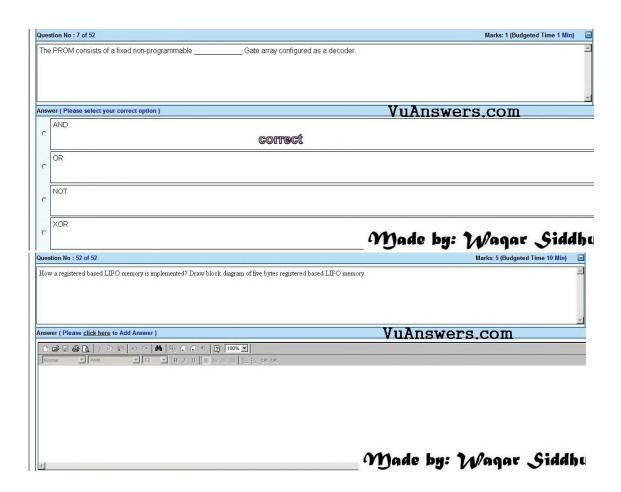
Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
The PROM consists of a fixed non-programmable Gate a	array configured as a decoder.
Answer (Please select your correct option)	VuAnswers.com
AND	V driib#CI b.COm
C	correct
OR	933 B 90 870 KKB
c	
NOT	
c	
XOR	
c	Made by: Wagar Siddh
0	
Question No : 38 of 52	Marks: 1 (Budgeted Time 1 Min)
The process of converting the analogue signal into a digital representation (code) is	known as
Answer (Please select your correct option)	VuAnswers.com
Strobing	
Amplification	
Quantization	
	correct
Digitization	
0	Made by: Waqar Siddh
Question No : 39 of 52	Marks: 1 (Budgeted Time 1 Min)
Sampling of an analog signal produces:	
Statipling of an analog signal produces.	
Annual Diagram alast usus assess tration)	Vu Anguong gom
Answer (Please select your correct option) A series of impulses those are proportional to the frequency of the signal	VuAnswers.com
A series of impulses mose are proportional to the frequency of the signal	
A series of impulses those are proportional to the amplitude of the signal	
Digital codes that represent the analog signal amplitude	
Digital codes that represent the time of each sample	
C	Made bu: 14/00ar Siddh











(Paper 3)

Question No : 1 of 52			Marks: 1 (Budg	eted Time 1 Min)
Excess-8 code assigns to "-8"				_
Answer (Please select your correct option)		VuAnav	vers.com	×
1110		Velian	VELS.COM	
1100				
1000				
c 0000	correct	Made by	j: Wagar	Siddh
Question No : 2 of 52				eted Time 1 Min)
The Extended ASCII Code (American Standard Code for Information Interchange)	represents ur	nique codes		
Answer (Please select your correct option)		VuAnsv	vers.com	
correct				
255				
c 128				
127 C				~~~
		Made by	j: Waqar	Siddh
Question No : 3 of 52			Marks: 1 (Budg	eted Time 1 Min)
The 3-variable Karnaugh Map (K-Map) has cells for min or max terms				
Answer (Please select your correct option)		Vulancy	vers.com	_
c 4		¥ 021115¥	VCI D.COM	
c 8				
12 C				
16				
C	rect	Made by	: Wagar	Siddh

Question No : 4 of 52	Marks: 1 (Budgeted Time 1 Min)
The active high and active low inputs of 3-to-8 Decoder are as follows:	<u> </u>
Answer (Please select your correct option)	VuAnswers.com
One active-high and the remaining two are active-low.	correct
Two active-high and the remaining one is active-low.	
C All active high	
All active low	Made by: Waqar Siddh
Question No : 5 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer { Please select your correct option }	VuAnswers.com
C 2-input, 4-bit 4-input, 8-bit	
4-input, 18-bit	
C 2-input, 8-bit CONTING	Made by: Waqar Siddh
Question No : 6 of 52	Marks: 1 (Budgeted Time 1 Min)
GAL is an acronym for	
Answer (Please select your correct option)	VuAnswers.com
Generic Analysis Logic	7 44444 11 44 44 44 44 44 44 44 44 44 44
Giant Array Logic	
General Array Logic	
Generic Array Logic	oct Made bu: 11/2001 Siddh

Ques	stion No : 7 of 52				Marks: 1 (Budget	ed Time 1 Min)
74H	IC163 has two enable input pins which are and					<u> </u>
Answ	ver (Please select your correct option)		VuAn	swe	rs.com	×
0	ENP, ENT	correct				
c	ENI, ENC					
0	ENP, ENC					
c	ENT, ENI		Made	by:	Wagar	Siddhu
Ques	stion No : 8 of 52				Marks: 1 (Budget	ed Time 1 Min) 🔳
A.(E	3 + C) = A B + A C is an expression of					<u> </u>
Answ	ver (Please select your correct option)		VuAn	swe	rs.com	
c	Demorgan's Law					
c	Commutative Law					
С	Distributive Law	orrect				
С	Associative Law		Made	by:	Wagar	Siddhu
Ques	stion No : 9 of 52				Marks: 1 (Budget	ed Time 1 Min) 🔳
An 8	8-bit serial in / parallel out shift register contains the value "8", clock sign	al(s) will be required to shift	the value completely out of the re	gister.		<u>^</u>
Answ	ver (Please select your correct option)		VuAn	swe	rs.com	<u> </u>
c	1 GOI	rrect				
0	2					
c	4					
c	8		Made	bи:	Magar	Siddhu

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	<u></u>
A (D t	V-A
Answer (Please select your correct option)	VuAnswers.com
EMP, ENT CONTOCT	
ENI, ENC	
ENP, ENC	
ENT, ENI	Made by: Wagar Siddhu
Question No : 11 of 52	Marks: 1 (Budgeted Time 1 Min)
The device shown here is most likely a	
Answer (Please select your correct option)	VuAnswers.com
Comparator	Vuanswers.com
C Multiplexer C COTTO	oct
C Demultiplexer	
Parity generator	Made by: Wagar Siddhu
Question No : 12 of 52	Marks: 1 (Budgeted Time 1 Min)
What will be output state when $J=1,K=0$ and CLR input is active?	A
Answer (Please select your correct option)	VuAnswers.com
${\sf C}$	
Q=0	
Retains previous output state	
Toggle output	Made by: Magar Siddho

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	2
Answer (Please select your correct option)	VuAnswers.com
C ENP, ENT	correct
ENI, ENC	
C ENP, ENC	
ENT, ENI	Made by: Wagar Siddh
Question No : 14 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option) Synchronous	VuAnswers.com
Asynchronous	correct
C Positive-Edge triggered	
Negative-Edge triggered	Made by: Wagar Siddh
Question No : 15 of 52	Marks: 1 (Budgeted Time 1 Min)
is said to occur when multiple internal variables change	due to change in one input variable.
Answer (Please select your correct option)	VuAnswers.com
C Race condition	correct
Propagation delay	
Ripple effect	
Clock skew	Made by: Magar Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	2
Answer (Please select your correct option)	VuAnswers.com
C ENP, ENT COFFECT	V 433222 V 42 27 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
c ENI, ENC	
ENP, ENC	
C ENT, ENI	Made by: Wagar Siddhu
Question No : 17 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option) C Moore Machine	VuAnswers.com
Mealy Machine Counter	
C Flip Flop	
	Made by: Wagar Siddho
Question No : 18 of 52	Marks: 1 (Budgeted Time 1 Min)
In, the $\overline{\mathbb{Q}}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flow.	flop.
Answer (Please select your correct option)	VuAnswers.com
C Moore machine	
C Mealy machine	
Johnson counter	
Ring counter COPPO	Made by: Wagar Siddhu

Ques	tion No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min)
74H	C163 has two enable input pins which are and				A
Answ	er (Please select your correct option)	VuAn	swe	rs.com	₩.
c	enp, ent coitisct				
0	ENI, ENC				
0	ENP, ENC				
0	ent, eni	Made	by:	Waqar	Siddh
Ques	tion No : 20 of 52			Marks: 1 (Budge	ted Time 1 Min)
The	minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _				A
Answ	er (Please select your correct option)	VuAn	swe	rs.com	<u>*</u>
С	Pulse Stability time (PST)				
О	Set-up time				
0	Hold time				
0	Pulse Interval time	Made	by:	Wagar	Siddh
Ques	tion No : 21 of 52			Marks: 1 (Budge	ted Time 1 Min)
RCG	Stands for				A
Answ	er (Please select your correct option)	VııAn	SWE	rs.com	<u> </u>
С	Reconfiguration Counter Output	* 42111		1.00m	
0	Reconfiguration Clock Output				
0	Ripple Counter Output				
0	Ripple Clock Output	Made	ри:	Magar	Siddho

Question No: 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	2
Answer (Please select your correct option)	VuAnswers.com
ENP, ENT	rrect
c ENI, ENC	
C ENP, ENC	
C ENT, ENI	Made by: Wagar Siddh
Question No : 23 of 52	Marks: 1 (Budgeted Time 1 Min)
	<u> </u>
Answer (Please select your correct option)	VuAnswers.com
C Moore Machine	orrect
Mealy Machine	
Counter	
Flip Flop	Made by: Waqar Siddh
Question No : 24 of 52	Marks: 1 (Budgeted Time 1 Min)
State Machine is a generic name given to	
Answer (Please select your correct option)	VuAnswers.com
C Sequential circuits	correct
Combinational circuits	
Flip-flops	
Counters	Made by: 14/200 Siddh

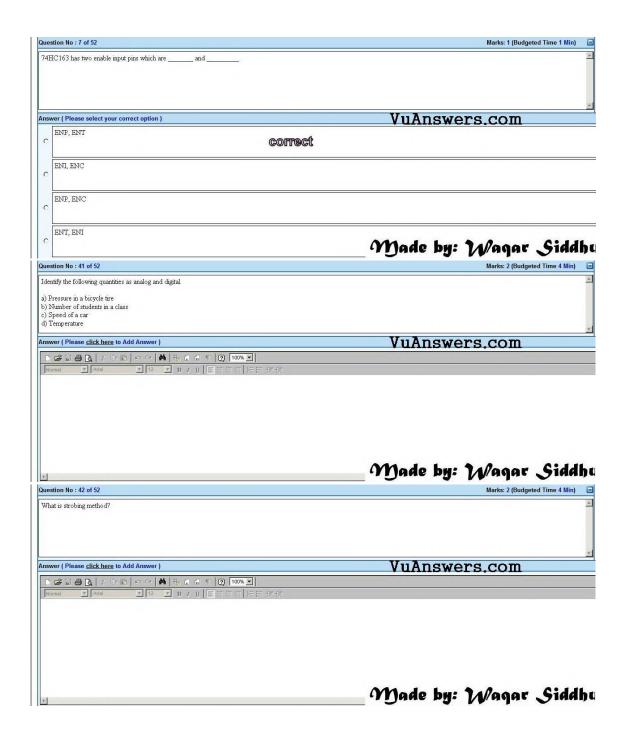
Question No : 7 of 52			Marks: 1 (Budge	eted Time 1 Min) 🔳
74HC163 has two enable input pins which are and	e .			A
Answer (Please select your correct option)		VuAnswe	ers.com	×
C ENP, ENT	correct			
ENI, ENC				
C EMP, EMC				
ENT, ENI		Made by:	Wagar	Siddho
Question No : 26 of 52			Marks: 1 (Budge	eted Time 1 Min) 🔳
Answer (Please select your correct option) State diagram		VuAnswe	ers.com	×
Next state table				
State reduction				
State assignment	correct	Made by:	Wagar	Siddhu
Question No : 27 of 52			Marks: 1 (Budge	eted Time 1 Min) 🔳
The output of this circuit is always +Vcc				_
Answer (Please select your correct option)		VuAnswe	na aom	J
T C		VUAIISW	ers.com	
0				
c A	correct			
c A		Made by:	Wagar	Siddhu

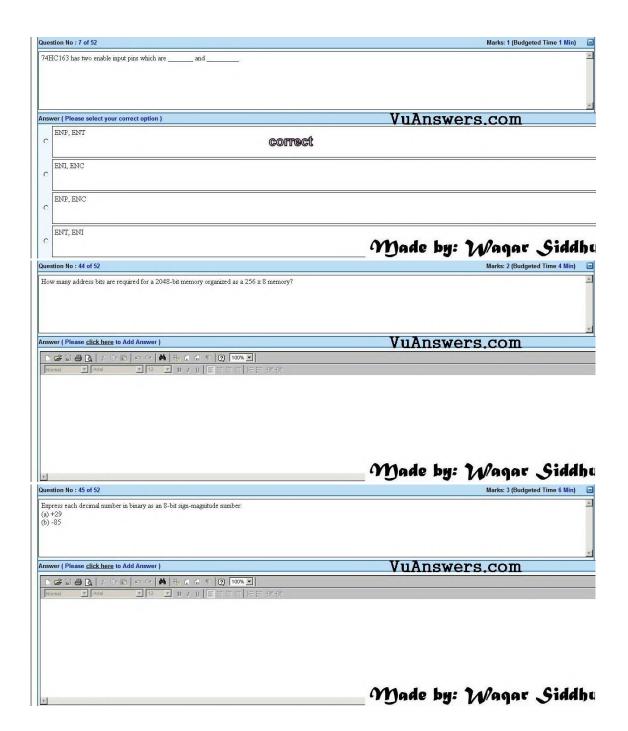
Question No: 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	
Answer (Please select your correct option)	VuAnswers.com
c Enp, ent contect	
ENI, ENC	
C ENP, ENC	
ENT, ENI	Made by: Wagar Siddh
Question No : 29 of 52	Marks: 1 (Budgeted Time 1 Min)
Which is not characteristic of a shift register?	<u>*</u>
Answer (Please select your correct option)	VuAnswers.com
Serial in/parallel in COFFECT	
C Serial in/parallel out	
C Parallel in/serial out	
Parallel in/parallel out	Made by: Waqar Siddh
Question No : 30 of 52	Marks: 1 (Budgeted Time 1 Min)
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. Wh	at will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)
Answer (Please select your correct option)	VuAnswers.com
C 1100	V drillb woll b.com
0000	
correct	
0 1111	Made bu: Magar Siddh

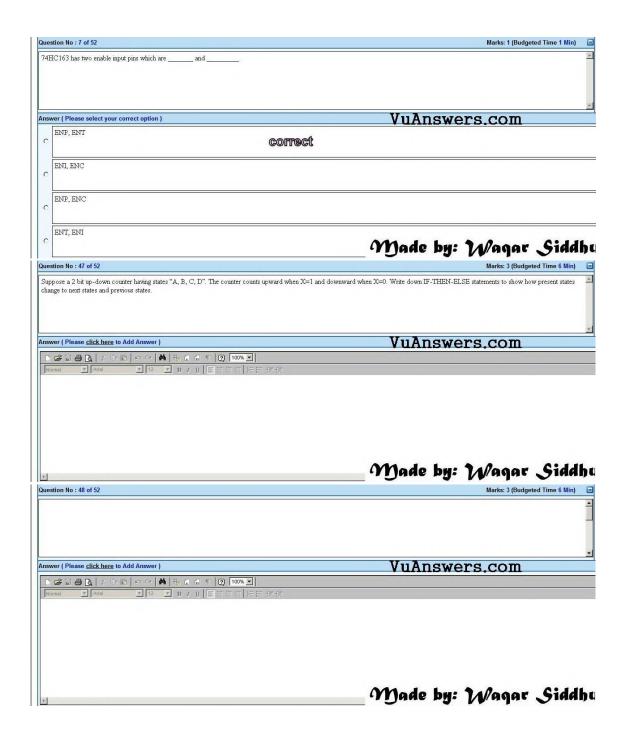
Question No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min)
74HC163 has two enable input pins which are and				<u> </u>
Answer (Please select your correct option)		VuAnswe	rc com	<u>, </u>
ENP, ENT		AUVIIPAG	LS.COIII	
0	correct			
ENI, ENC				
ENP, ENC				
C ENT, ENI		Made by:	Wagar	Siddh
Question No : 32 of 52			Marks: 1 (Budge	ted Time 1 Min)
Smallest unit of binary data is a				
Answer (Please select your correct option)		VuAnswe	rs.com	<u> </u>
C Bit	correct			
C Nibble				
Byte				
Word		Made by:	Wagar	Siddh
Question No : 33 of 52			Marks: 1 (Budge	ted Time 1 Min)
The of a ROM is the time it takes for the data to appear at the I Output of the ROM chip after an address is applied at the address input lines				2
Answer (Please select your correct option)		VuAnswe	rs.com	<u> </u>
C Write Time				
Refresh Time				
Refresh Time				
Access Time	correct	Made by:	Magar	Siddh

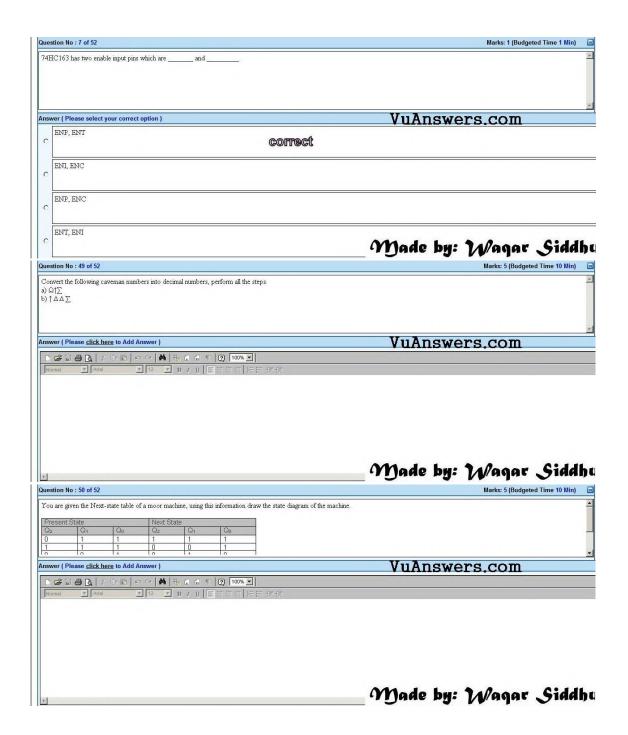
Question No: 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	2
Answer (Please select your correct option)	VuAnswers.com
C ENP, ENT	correct
ENI, ENC	
ENP, ENC	
ENT, ENI	Made by: Wagar Siddh
Question No : 35 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
The size of the address bus of the microprocessor	correct
The organization of memory	
The structure of memory	
The size of decoding unit ${\cal C}$	Made by: Wagar Siddh
Question No : 36 of 52	Marks: 1 (Budgeted Time 1 Min)
The voltage gain of the Inverting Amplifier is given by the relation	
Answer (Please select your correct option)	VuAnswers.com
$V_{out}/V_{in} = -R_f/R_i$	
$V_{out} / R_f = -V_{in} / R_i$	Correct
0	
$C = \frac{R_{\rm d}/V_{\rm in} = -R_{\rm d}/V_{\rm out}}{R_{\rm d}/V_{\rm in}}$	
C $R_{\ell}/V_{in} = R_{i}/V_{out}$	Made hu: 14/2021 Siddh

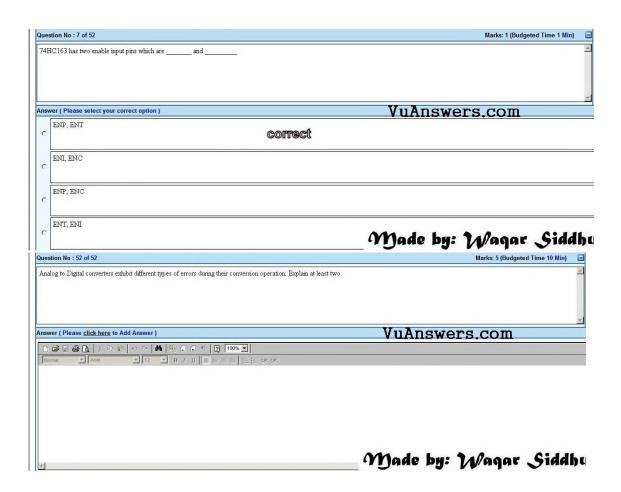
Ques	ion No : 7 of 52		Marks: 1 (Budge	eted Time 1 Min)
74H	C163 has two enable input pins which are and			A
Answ	er (Please select your correct option)	VuAnsw	ers.com	<u>~</u>
С	enp, ent coitect			
c	ENI, ENC			
c	ENP, ENC			
0	ENT, ENI	Made by:	: Wagar	Siddhu
Ques	ion No : 38 of 52		Marks: 1 (Budge	eted Time 1 Min)
A fla	sh A/D converter uses :			<u>*</u>
Answ	er (Please select your correct option)	VuAnsw	ers com	<u> </u>
О	Counters	¥ 42111D#	orb.com	
c	Flip-flops			
С	Op-amps COITICE			
c	An integrator	Made by	: Wagar	Siddhu
Ques	ion No : 39 of 52		Marks: 1 (Budge	ted Time 1 Min)
	of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.			<u>*</u>
Answ	er (Please select your correct option)	VuAnsw	ers com	
С	Resolution	, <u> </u>	D, OVIII	
c	Accuracy COFFECT			
С	Quantization			
c	Missing Code	Made bu	Magar	Siddhu











(Paper 4)

Question No : 1 of 52	Marks: 1 (Budgeted Time 1 Min)
The hexadecimal value "FD" is equivalent to binary value	<u>a</u>
	×
Answer (Please select your correct option)	VuAnswers.com
c 110111111	
11111101 ©©	prrect
c 11001110	
C 00010111	Made by: Wagar Siddho
Question No : 2 of 52	Marks: 1 (Budgeted Time 1 Min)
A+B=B+A is	·
Answer (Please select your correct option)	VuAnswers.com
C Demorgan's Law	
Distributive Law	
C Commutative Law	
Associative Law	Made by: Wagar Siddhu
Question No : 3 of 52	Marks: 1 (Budgeted Time 1 Min)
is invalid number of cells in a single group formed by the adjacent cells in K-map	<u>*</u>
Answer (Please select your correct option)	VuAnswers.com
c ²	Value wells (com
8	
c 12 COITIS	ct
С 18	Made by: Wagar Siddhu

Question No : 4 of 52			Marks: 1 (Budgeted Time 1 Min)
The Encoder is used as a keypad encoder.			
		W 7	
nswer (Please select your correct option)		VuAnswers	.COIII
2-to-8 encoder			
4-to-16 encoder			
BCD-to-Decimal			
Decimal-to-BCD Priority	correct	Made by: N	Pagar Siddh
tuestion No : 5 of 52			Marks: 1 (Budgeted Time 1 Min)
The Programmable Array Logic (PAL) has AND array and a	a OR array		
nswer (Please select your correct option)		VuAnswers	.com
Fixed, programmable			
Programmable, fixed	0.0770.04		
	correct		
Fixed, fixed			
Programmable, programmable		244 1 1 4	
		Made by: U	/agar Sidal
Question No : 6 of 52			Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and			
		W-2	
Answer (Please select your correct option)		VuAnswers	.com
ENP, ENT	orrect		
ENI, ENC			
ENP, ENC			
ENT, ENI		Mada kas As	
		Made by: U	pagar Siaa

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
	VuAnswers.com
nswer (Please select your correct option)	V UAIISWELS, COIII
The next state of a given present state	correct
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Wagar Siddl
uestion No : 8 of 52	Marks: 1 (Budgeted Time 1 Min)
	signal(s) will be required to shift the value completely out of the register (i.e. to set the register to 0).
nswer (Please select your correct option)	VuAnswers.com
c 1	
2 3	CONTRCT
C 4	Made by: Waqar Siddl
Question No : 9 of 52	Marks: 1 (Budgeted Time 1 Min)
In Single-Precision Floating Point format, "exponent" is represented by _	bits.
Answer (Please select your correct option)	VuAnswers.com
c 8-bits	
18-bits	
C 32-bits	correct
C 64-bits	Made by: Wagar Siddl

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Wagar Siddl
Question No : 11 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
	VUAIISWELS,COIII
C Single, multiple	
Multiple, single	
Single, single	
Multiple, multiple CONTROCT	Made by: Wagar Siddl
Question No : 12 of 52	Marks: 1 (Budgeted Time 1 Min)
At S = 0 and R = 1, an active-HIGH SR latch is in condition.	
nswer (Please select your correct option)	VuAnswers.com
SET	
RESET CONTROCT	not sure
C Invalid	
C No change	Made by: Waqar Siddl

Question No : 7 of 52			Marks: 1 (Budge	eted Time 1 Min)
Given the state diagram of an up/down counter, we can find				
inswer (Please select your correct option)		VuAnswe	ers.com	
The next state of a given present state	correct			
The previous state of a given present state				
Both the next and previous states of a given state				
The state diagram shows only the inputs/outputs of a given states		Made by:	Waqar	Siddh
luestion No : 14 of 52			Marks: 1 (Budge	eted Time 1 Min)
The negative edge triggered flip-flop changes state on				
nswer (Please select your correct option)		VuAnswe	rs.com	
Positive half cycle of clock		V GIIIIOW G	10,0011	
Negative half of clock				
Low-to-high transition of clock				
High-low transition of clock	correct	Made by:	Waqar	Siddh
Question No : 15 of 52			Marks: 1 (Budge	eted Time 1 Min)
When four 1's are taken as a group on a Karnaugh map, the number of wa	riables eliminated from the output express	ion is/are		
nswer (Please select your correct option)		VuAnswe	ers.com	
·				
c 2				
c 3				
C 4	correct	Made by:	Wagar	Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	V driiibwci b,com
c	Contract
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Waqar Siddl
uestion No : 17 of 52	Marks: 1 (Budgeted Time 1 Min)
nswer (Please select your correct option)	VuAnswers.com
C Truth table	
K-map	
C State table	
C State diagram	rroct Made by: Waqar Siddl
Question No : 18 of 52	Marks: 1 (Budgeted Time 1 Min)
The best state assignment tends to	
Answer (Please select your correct option)	VuAnswers.com
Maximizes the number of state variables that don't change in a group of related states	correct
Minimizes the number of state variables that don't change in a group of related states	
Minimizes the equivalent states	
Maximizes the equivalent states	Made by: Waqar Siddl

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	rrect
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Wagar Siddl
Question No : 20 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
Moore machine	T dillion of D. Coll
0	
Mealy machine	
Johnson counter COFFSCT	
Ring counter	Made by: Wagar Siddl
Question No : 21 of 52	Marks: 1 (Budgeted Time 1 Min)
If S=1 and R=0, then $Q(t+1) = \underline{\hspace{1cm}}$ for positive edge triggered flip-flop	
Answer (Please select your correct option)	VuAnswers.com
0	
Tanvalid COFFECT	
Input is invalid	
Input is myand	Made by: Wagar Sidd

uestion No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	correct
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Waqar Sidd
estion No : 23 of 52	Marks: 1 (Budgeted Time 1 Min)
Thich of the following is NOT a sequential circuit?	
nuar / Places relect your servest entire)	VuAnswers.com
swer (Please select your correct option) SR latch	V UAIISWELS,COIII
Counter COUNTER	rect
Full Adder	
ЈК Flip-flop	Made by: Waqar Sidd
estion No : 24 of 52	Marks: 1 (Budgeted Time 1 Min)
ach stage of Master-slave flip-flop works in	
swer (Please select your correct option)	VuAnswers.com
One complete clock signal	
One fourth of the clock signal	
One third of the clock signal	
One half of the clock signal	correct Made by: Waqar Sidd

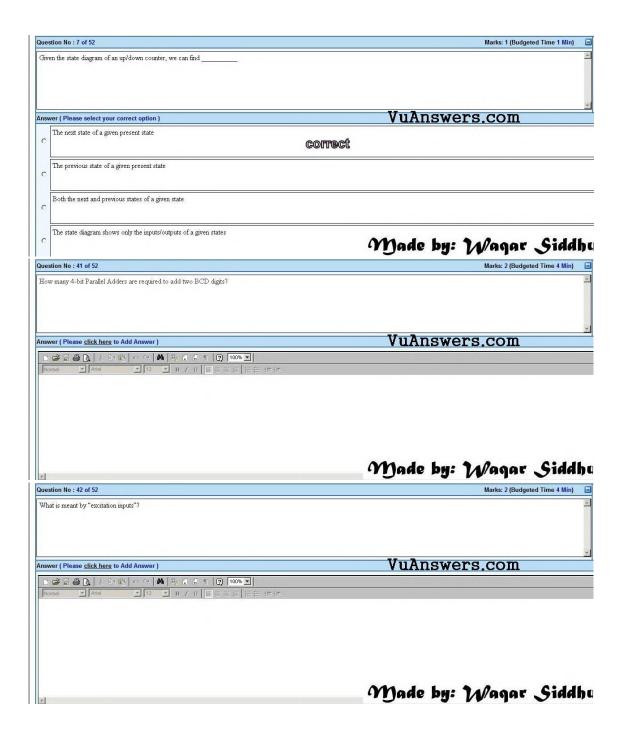
Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	correct
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Wagar Siddl
Question No : 26 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option) Reconfiguration Counter Output	VuAnswers.com
Reconfiguration Clock Output	
Ripple Counter Output Ripple Clock Output	
	correct Made by: Wagar Siddl
A divide-by-50 counter divides the input signal to a 1 Hz signal.	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
C 10 Hz	
C SO Hz COM	rect
C 100 Hz	
C 500 Hz	Made by: Waqar Siddl

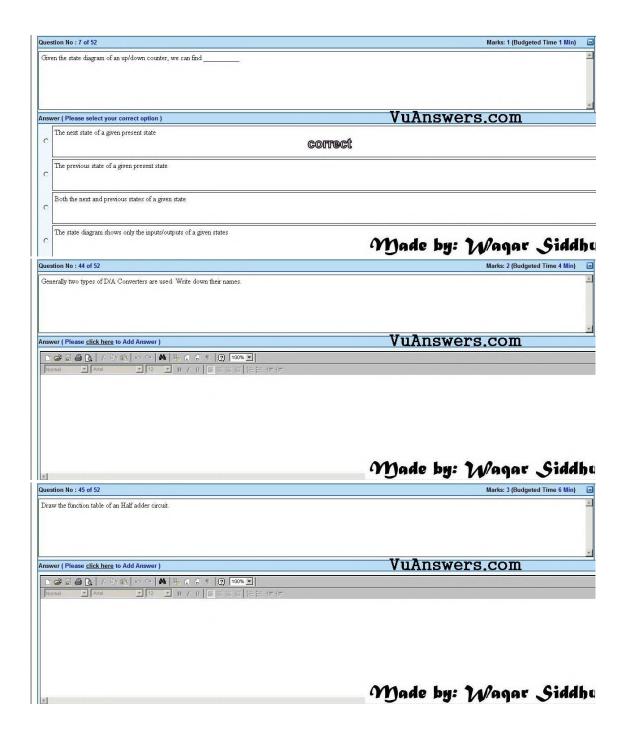
uestion No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	Vuniiswei s.com
	correct
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Wagar Sidd
uestion No : 29 of 52	Marks: 1 (Budgeted Time 1 Min)
n asynchronous transmission when the transmission line is idle,	
iswer (Please select your correct option)	VuAnswers.com
It is set to logic low	V UMIISWELS,COIII
It is set to logic high	=
Remains in previous state	
O New Contract Contraction	
State of transmission line is not used to start transmission	
	Made by: Wagar Sidd
uestion No : 30 of 52	Marks: 1 (Budgeted Time 1 Min)
he output of this circuit is always	mans. I (budgeted fille i mill)
`	
÷	
swer (Please select your correct option)	VuAnswers.com
1	
0	
Correct	
Ā	
A A	Made by: Wagar Sidd

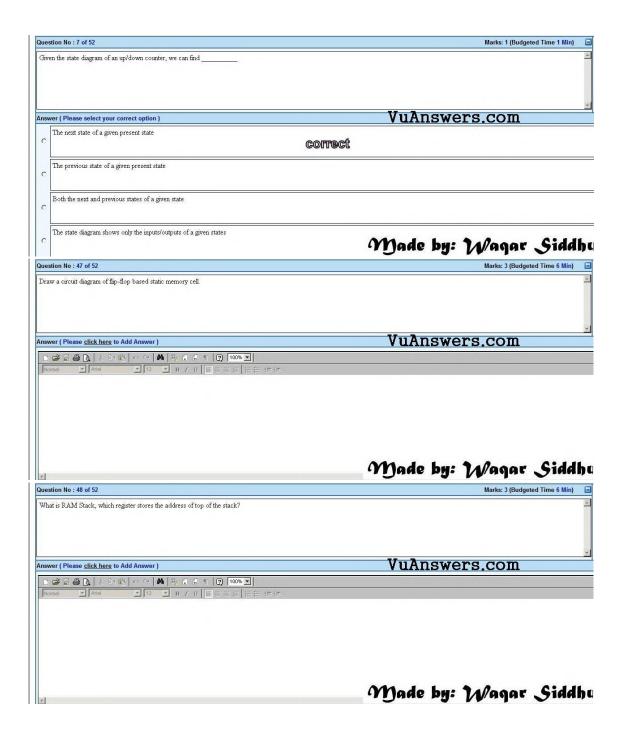
luestion No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	2.000 (a)
	Contract
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Waqar Siddh
uestion No : 32 of 52	Marks: 1 (Budgeted Time 1 Min)
nswer (Please select your correct option)	VuAnswers.com
2	V UAIISWELS,COIII
c	
c 4 COI	rrect
c 8	
c 16	Made by: Waqar Siddh
uestion No : 33 of 52	Marks: 1 (Budgeted Time 1 Min)
The of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines	
nswer (Please select your correct option)	VuAnswers.com
Write Time	v driiibwor b,oom
Refresh Time	
Refresh Time	
Access Time	orroct Made by: Waqar Siddh

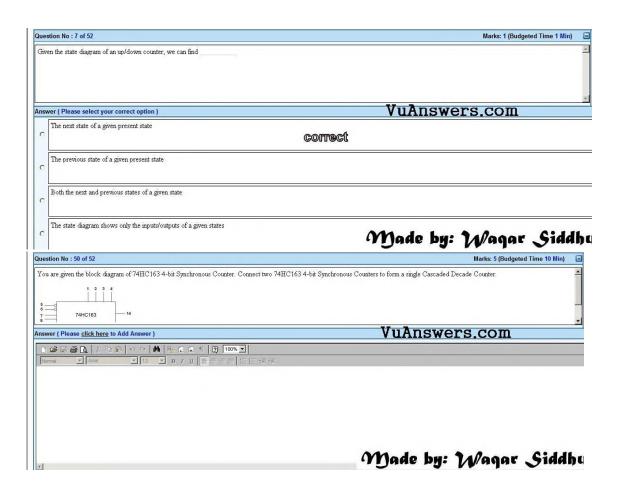
Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
nswer (Please select your correct option)	VuAnswers.com
The next state of a given present state	V driibwerb.com
	correct
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Magar Siddl
Question No : 35 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
C Read Only Memory	
First In First Out Memory	prect
Flash Memory	
Fast Page Access Mode Memory	Made by: Waqar Siddl
Question No : 36 of 52	Marks: 1 (Budgeted Time 1 Min)
The process of converting the analogue signal into a digital representation (code) is known as	
Answer (Please select your correct option)	VuAnswers.com
Strobing	
Amplification	
Quantization COTTEC	The state of the s
C Digitization	Made by: Waqar Siddl

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
Given the state diagram of an up/down counter, we can find	
Answer (Please select your correct option)	VuAnswers.com
The next state of a given present state	V daiiswet s.com
	orrect
The previous state of a given present state	
Both the next and previous states of a given state	
The state diagram shows only the inputs/outputs of a given states	Made by: Waqar Siddl
Question No : 38 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
Counters	
Fip-Bops	
C Op-amps COTTOC	
An integrator	Made by: Waqar Siddl
Question No : 39 of 52	Marks: 1 (Budgeted Time 1 Min)
of a D/A converter is determined by comparing the actual output of a D/A converter with the e	xpected output.
Answer (Please select your correct option)	VuAnswers.com
Resolution C	
Accuracy COMPCT	
Quantization	
Missing Code	Made by: Waqar Siddl











(Paper 5)

Question No : 1 of 52	Marks: 1 (Budgeted Time 1 Min)
Cavernan number system is Base number system	<u> </u>
	×
Answer (Please select your correct option)	VuAnswers.com
2	
5 CONTRCT	
c 10	
	Made by: Waqar Siddhi
Question No : 2 of 52	Marks: 1 (Budgeted Time 1 Min)
110 / 10 =	_
Note: both values are in binary	
	VuAnswers.com
Inswer (Please select your correct option)	Vualiswers.com
correct	
10	
C T	
111	
C	
101	
C	Made by: Wagar Siddh
Question No : 3 of 52	Marks: 1 (Budgeted Time 1 Min)
The circuit diagram below explains the	<u> </u>
A A+(B+C) A	
B AHB	
B (A+B)+C	
inswer (Please select your correct option)	VuAnswers.com
Associative Law for Multiplication	
Commutative Law for Addition	
Commutative Law for Multiplication	
Associative Law for Addition	6 Mada bur \$40aaaa Cilib
COFFEC	Made by: Wagar Siddh

For More Visit VU Answer

	1 No : 4 of 52		Marks: 1 (Budge	ted Time 1 Min)
A + Ā.I	3=			
Inswer	Please select your correct option)	VuAnswe	ers.com	
A				
СВ				
C A.I	В			
L				
C A+	correct	Made by:	14/000	Ciddh
	1 20 40 1 1 2 40 2	. Dane pg.		
uestion	1 No : 5 of 52		Marks: 1 (Budge	ted Time 1 Min)
ĀB + Ā	BC + AC is an example of			4
				•
nswer	Please select your correct option)	VuAnswe	ers.com	
Pri	oduct of sum form			
Su	m of product form			
	correct			
De	morgans law			
As C	sociative law	MA . J . L		A. 111.
		Made by:	Madar	Sigan
uestion	No: 6 of 52		Marks: 1 (Budge	ted Time 1 Min)
A stand	lard POS form hasterms that have all the variables in the domain of the expression.			<u> </u>
				▼
nswer	Please select your correct option)	VuAnswe	ers.com	
Su				
	Correct			
Pri	oduct			
Mir	1			
0				
	mposite			1202 Marian
0		Made bu:	Magar	Siddh

Question No : 7 of 52			Marks: 1 (Budge	eted Time 1 Min)
74HC163 has two enable input pins which are and				2
Answer (Please select your correct option)		VuAnswe	ers.com	
ENP, ENT				
0	correct			
ENI, ENC				
ENP, ENC				
ENT, ENI		Made by:	Wagar	Siddh
Question No : 8 of 52			Marks: 1 (Budge	ted Time 1 Min)
Given the state diagram of an up/down counter, we can find				
Answer (Please select your correct option)		VuAnswe	ers.com	
The next state of a given present state	correct			
The previous state of a given present state				
Both the next and previous states of a given state				
The state diagram shows only the inputs/outputs of a given s	states	Made by:	Wagar	Siddh
Question No : 9 of 52			Marks: 1 (Budge	ted Time 1 Min)
A multiplexer with a register circuit converts				*
Answer (Please select your correct option)		VuAnswe	ers.com	
Serial data to parallel				
Parallel data to serial	correct			
Serial data to serial				
Parallel data to parallel		Made bu:	14/99gr	Siddh

Question No : 7 of 52			Marks: 1 (Budge	eted Time 1 Min)
74HC163 has two enable input pins which are and				
inswer (Please select your correct option)		VuAnsw	ers.com	
ENP, ENT				
	correct			
ENI, ENC				
ENP, ENC				
ENT, ENI				
С		Made by	: Wagar	Siddh
Question No : 11 of 52			Marks: 1 (Budge	eted Time 1 Min)
Answer (Please select your correct option)		VuAnsw	ers.com	-
Output of flip-flop will be set (Logic 1)				
0	correct			
Output of flip-flop will be reset (Logic 0)				
Output of flip-flop will be invalid				
Flip-flop will change output on Clock transition		Made by	: Wagar	Siddh
Question No : 12 of 52			Marks: 1 (Budge	eted Time 1 Min)
Compared to analog systems, digital systems	į.			_
Answer (Please select your correct option)		VuAnsw	ers.com	
are less prone to noise	correct		not s	sure
can represent an infinite number of values				
can handle much higher power				
occupy large space		Made bu	: 14/200r	Ciddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	
answer (Please select your correct option)	VuAnswers.com
ENP, ENT	Variibwerb.com
c	correct
C ENI, ENC	
ENP, ENC	
ENT, ENI	Made by: Waqar Siddh
Question No : 14 of 52	Marks: 1 (Budgeted Time 1 Min)
inswer (Please select your correct option) $A = 1, B = 0, C = 0, D = 0$	VuAnswers.com
A=1,B=0,C=1,D=0 A=0,B=1,C=0,D=1	correct
C A=1, B=0, C=1, D=1	Made by: Waqar Siddh
Luestion No : 15 of 52 Determine the values of A , B , C , and D for the product term $ABCO$	Marks: 1 (Budgeted Time 1 Min)
Innuer I Blaze releat usur correct cettics I	VuAnswers.com
Answer (Please select your correct option) A = 0, B = 1, C = 0, D = 1	¥ UAII3WEL 5.COIII
C X-0, B-1, C-0, B-1	correct
A=1, B=0, C=1, D=0	
A=1, B=1, C=1, D=1	
A = 0, B = 0, C = 1, D = 0	Made by: Wagar Siddh

Question No : 7 of 52			Marks: 1 (Budge	ted Time 1 Min)
74HC163 has two enable input pins which are and				2
Answer (Please select your correct option)		VuAnswe	rs com	
ENP, ENT		V GIIIID W C	DI D.COM	
C	correct			
ENI, ENC				
ENP, ENC				
ENT, ENI		Made by:	Waqar	Siddh
Question No : 17 of 52			Marks: 1 (Budge	
Answer (Please select your correct option)		VuAnswe	ers.com	<u> </u>
Truth table K-map State table				
State diagram		244 1 1		0.11
	correct	Made by:	Wagar	Staan
Question No : 18 of 52	8.8 9 40		Marks: 1 (Budge	ted Time 1 Min)
The Sequential circuit whose output depends on the current state and	d the input is known as			
Answer (Please select your correct option)		VuAnswe	rs com	
Moore Machine		, dillipwe	25.00m	
Mealy Machine	correct			
Counter				
C Flip Flop		Made bu:	Magar	Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	<u> </u>
Answer (Please select your correct option)	VuAnswers.com
ENP, ENT	V drills word, com
0	correct
C ENI, ENC	
ENP, ENC	
C ENT, ENI	Made by: Waqar Siddh
Question No : 20 of 52	Marks: 1 (Budgeted Time 1 Min)
	ister is connected to the data input of the first flip-flop of the shift register.
Answer (Please select your correct option) Moore machine	VuAnswers.com
Mealy machine	
Johnson counter	a a manach
	correct
C Ring counter	Made by: Wagar Siddh
Question No : 21 of 52	Marks: 1 (Budgeted Time 1 Min)
Invalid state of NOR based SR latch occurs when	
Answer (Please select your correct option)	VuAnswers.com
C S=0, R=0 C S=0, R=1	V GIIID WOLD, GOIL
S=1, R=0	
C S=1, R=1	correct Made by: 14/agar Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	
nswer (Please select your correct option)	VuAnswers.com
C ENP, ENT	rrect
ENI, ENC	
ENP, ENC	
ENT, ENI	Made by: Waqar Siddh
uestion No : 23 of 52	Marks: 1 (Budgeted Time 1 Min)
Following is the circuit diagram of mono-stable device. Which gate will be replaced	by the red colored rectangle in the circuit?
+V	
Š p	
C }"	
nswer (Please select your correct option)	VuAnswers.com
C AND	
XIVOR	correct
NAND	
NOR	Made by: Waqar Siddh
uestion No : 24 of 52	Marks: 1 (Budgeted Time 1 Min)
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation	on, the power dissipation of the flip-flop is
nswer (Please select your correct option)	VuAnswers.com
10 mW	V dimbwoi b.com
C 25 mW	correct
C 64 mW	
c 84 mW	Made by: Magar Siddh

Question No : 7 of 52	Marks: 1	(Budgeted Time 1 Min)
74HC163 has two enable input pins which area	and	<u> </u>
nswer (Please select your correct option)	VuAnswers.com	m.
ENP, ENT	and amount	as reads seems
	correct	
C ENI, ENC		
ENP, ENC		
ENT, ENI	Made by: Waq	ar Siddh
Question No : 26 of 52	Marks: 1	(Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com	m.
Moore Machine	correct	
Mealy Machine		
Counter		
C Flip Flop	Made by: Waq	ar Siddh
Question No : 27 of 52	Marks: 1	(Budgeted Time 1 Min)
In asynchronous transmission when the transmission line is	idle,	<u> </u>
Answer (Please select your correct option)	VuAnswers.com	m.
C It is set to logic low		
It is set to logic high	correct	
Remains in previous state		
State of transmission line is not used to start transmiss	Made bu: 148aa	ar Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and	2
Answer (Please select your correct option)	VuAnswers.com
The second secon	V UIIII SWEL S.COM
ENP, ENT COTTOCT	
C ENI, ENC	
C ENP, ENC	
C ENT, ENI	Made by: Waqar Siddh
Question No : 29 of 52	Marks: 1 (Budgeted Time 1 Min)
D — 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	<u>×</u>
Which of the following statement is true regarding above block diagram?	<u>, , , , , , , , , , , , , , , , , , , </u>
Answer (Please select your correct option)	VuAnswers.com
Triggering takes place on the negative-going edge of the CLK pulse	
Triggering takes place on the positive-going edge of the CLK pulse	correct
Triggering can take place anytime during the LOW level of the CLK waveform	
Triggering can take place anytime during the LOW level of the CLK waveform	Made by: Waqar Siddh
Question No : 30 of 52	Marks: 1 (Budgeted Time 1 Min)
Which is not characteristic of a shift register?	<u> </u>
Answer (Please select your correct option)	VuAnswers.com
Serial in/parallel in	
correct	
Serial in/parallel out	
Parallel in/serial out	
Parallel in/parallel out	Made by: Wagar Siddh

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and _	
nswer (Please select your correct option)	VuAnswers.com
ENP, ENT	V UALISWELS.COIII
C ENT, ENT	correct
ENI, ENC	
ENP, ENC	
ENT, ENI	Mada hu 14/2004 Ciddh
	Made by: Wagar Siddhi
uestion No : 32 of 52	Marks: 1 (Budgeted Time 1 Min)
nswer (Please select your correct option)	VuAnswers.com
Bit	correct
Nibble	
Byte	
Word	Made by: Wagar Siddhi
uestion No : 33 of 52	Marks: 1 (Budgeted Time 1 Min)
The high density FLASH memory cell is implemented using	
	· ·
nswer (Please select your correct option)	VuAnswers.com
1 floating-gate MOS transistor	correct
2 floating-gate MOS transistors	
4 floating-gate MOS transistors	
6 floating-gate MOS transistors	Made by: Magar Siddhe

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which area	d
Answer (Please select your correct option)	VuAnswers.com
ENP, ENT	Vullibwolb.com
C	correct
C ENI, ENC	
ENP, ENC	
C ENT, ENI	Made by: Waqar Sidd
Question No : 35 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option)	VuAnswers.com
Read Only Memory	
First In First Out Memory	correct
Flash Memory	
Fast Page Access Mode Memory	Made by: Wagar Sidd
Question No : 36 of 52	Marks: 1 (Budgeted Time 1 Min)
Stack is a	
Answer (Please select your correct option)	VuAnswers.com
Bust Flash Memory	
C FIFO memory	
C LIFO memory	correct
C Flash Memory	Made bu: 14/agar Sidd

Question No : 7 of 52	Marks: 1 (Budgeted Time 1 Min)
74HC163 has two enable input pins which are and _	
nswer (Please select your correct option)	VuAnswers.com
ENP, ENT	in demands
	correct
C ENI, ENC	
ENP, ENC	
ENT, ENI	Made by: Wagar Siddh
Question No : 38 of 52	Marks: 1 (Budgeted Time 1 Min)
Answer (Please select your correct option) Strobing	VuAnswers.com
Amplification	
Quantization	correct
Digitization	Made by: Wagar Siddh
Question No : 39 of 52	Marks: 1 (Budgeted Time 1 Min)
A hold action occurs :	
Answer (Please select your correct option)	VuAnswers.com
After the analog-to-digital conversion	
During each sample	
Immediately after a sample	correct
Before each sample	Made bu: 14/agar Siddhi

