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Divide binary number "1101" by binary number "101", write down all the steps.

Answer ( [Please click here to Add Answer](#) )

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Name the single change which can be made to convert a combinational circuit to a sequential circuit?

Answer ( [Please click here to Add Answer](#) )

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Write down the names of two basic operations which are performed on memory?

Answer ( [Please click here to Add Answer](#) )

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What is the function of row and column decoders?

Answer ( [Please click here to Add Answer](#) )

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Large memories such as the 16 KB memory have row and column decoders that split the input address into a row address and a column address and activate a row and column select lines respectively.

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Following two waves are applied at 2-input AND gate, Draw the output waveform of this gate.

A 

B 

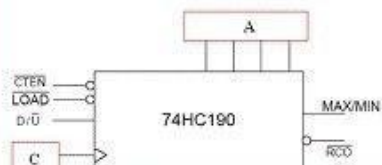
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You are given the block diagram of 74HC190 integrated circuit of 4-bit synchronous up/down counter, Name the pins which are under red boxes.



Answer ( [Please click here to Add Answer](#) )

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Write down three characteristics of serial in / serial out 4-bit left shift register.

Answer ( [Please click here to Add Answer](#) )

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Draw the circuit diagram of operational amplifier used as an inverting amplifier.

Answer ( [Please click here to Add Answer](#) )

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Convert the following Boolean expression into standard SOP form:

$$A\bar{B}C + \bar{A}\bar{B} + ABC\bar{D}$$

Answer ( [Please click here to Add Answer](#) )

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A rich text editor toolbar with various icons for text formatting and editing. It includes a dropdown menu for font style (currently set to 'Normal'), a dropdown for font face (currently set to 'Arial'), a dropdown for font size (currently set to '12'), and buttons for bold (B), italic (I), underline (U), bulleted list, numbered list, indent, and outdent. A zoom level dropdown is also present, currently set to '100%'.

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Draw the next-state table of a 3-bit Up Counter.

Answer ( [Please click here to Add Answer](#) )

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Draw a complete test vector table for a 3-bit up/down counter using the following information.

- X is excitation input (if  $X=0$ , counter counts upward and vice versa).
- When the Clear input is 0 the output is cleared to 000 irrespective of the X.
- When the Clear input is set to 1 counter functions normally.
- Clear, Clock and X are inputs for up-down counter.

Answer ( [Please click here to Add Answer](#) )

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Analog to Digital converters exhibit different types of errors during their conversion operation. Explain at least two.

Answer ( [Please click here to Add Answer](#) )

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Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations.

Answer ( [Please click here to Add Answer](#) )

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What is meant by state variable?

Answer ( [Please click here to Add Answer](#) )

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The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. What will be the contents of register after two clock pulses?

Answer ( [Please click here to Add Answer](#) )

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What is the function of row and column decoders?

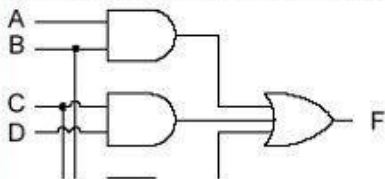
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From the circuit diagram given below derive the output expression.



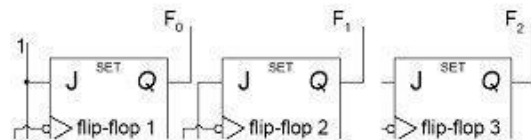
Answer ( [Please click here to Add Answer](#) )

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Following is an incomplete circuit of 3-bit Synchronous Down-counter, in which flip-flop 3 is left unconnected. Connect this 3<sup>rd</sup> flip-flop with flip-flop 2 in such a way that functionality of 3-bit Synchronous Down-counter is achieved.



Answer ( [Please click here to Add Answer](#) )

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Suppose a 2 bit up-down counter having states "A, B, C, D". The counter counts upward when  $X=1$  and downward when  $X=0$ . Write down IF-THEN-ELSE statements to show how present states change to next states and previous states.

Answer ( [Please click here to Add Answer](#) )

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How DRAMs are different from SRAMs? Write three point of differences.

Answer ( [Please click here to Add Answer](#) )

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Using K- map, minimize the following POS expression:

$$(A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)$$

Answer ( [Please click here to Add Answer](#) )

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Draw the state diagram of a 3-bit up-down counter. Use an external input  $X$ ; when  $X$  sets to logic 1, the counter counts downward otherwise counts upward.

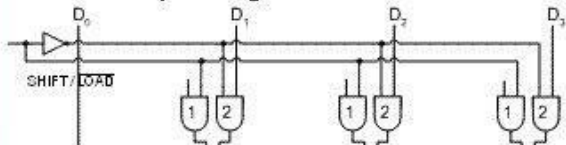
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Given below is an incomplete circuit diagram of parallel in / serial out shift register, in which  $Q_0$ ,  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and Clock input are disconnected. Connect above mentioned connections in such a way that functionality of the given circuit is not affected.



Answer ( Please [click here](#) to Add Answer )

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How a registered based LIFO memory is implemented? Draw block diagram of five bytes registered based LIFO memory.

Answer ( [Please click here to Add Answer](#) )

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Identify the following quantities as analog and digital.

- a) Pressure in a bicycle tire
- b) Number of students in a class
- c) Speed of a car
- d) Temperature

Answer ( [Please click here to Add Answer](#) )

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Write down any two applications of shift registers.

Answer ( [Please click here to Add Answer](#) )

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How many address bits are required for a 2048-bit memory organized as a 256 x 8 memory?

Answer ( [Please click here to Add Answer](#) )

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Express each decimal number in binary as an 8-bit sign-magnitude number:

(a) +29

(b) -85

Answer ( [Please click here to Add Answer](#) )

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How can we calculate the frequency of an unknown signal?

Answer ( [Please click here to Add Answer](#) )

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Made by: Waqar Siddhu

Suppose a 2 bit up-down counter having states "A, B, C, D". The counter counts upward when  $X=1$  and downward when  $X=0$ . Write down IF-THEN-ELSE statements to show how present states change to next states and previous states.

Answer ( [Please click here to Add Answer](#) )

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Answer ( Please [click here](#) to Add Answer )

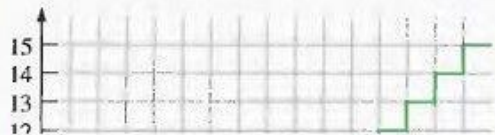
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Normal | Arial | 12 | B / I / U | [List icons] | [Link icon] | [Text color icon] | [Background color icon]

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A 4-bit flash A/D converter is tested for faults. The resulting reconstructed analog output is shown below. Identify the problem and the most probable reason due to which this fault is occurred.



Answer ( [Please click here to Add Answer](#) )

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Convert the following caveman numbers into decimal numbers, perform all the steps.

- a)  $\Omega\uparrow\Sigma$   
b)  $\uparrow\Delta\Delta\Sigma$

Answer ( [Please click here to Add Answer](#) )

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You are given the Next-state table of a moor machine, using this information draw the state diagram of the machine.

Present State			Next State		
Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	1	1	1	1	1
1	1	1	0	0	1
0	0	1	0	1	0

Answer ( [Please click here to Add Answer](#) )

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Normal Arial 12 B I U

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Make block diagram of Rotate Left Operation of a shift register and explain its working.

Answer ( [Please click here to Add Answer](#) )

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Analog to Digital converters exhibit different types of errors during their conversion operation. Explain at least two.

Answer ( [Please click here to Add Answer](#) )

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How many 4-bit Parallel Adders are required to add two BCD digits?

Answer ( [Please click here to Add Answer](#) )

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What is meant by "excitation inputs"?

Answer ( [Please click here to Add Answer](#) )

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How many bytes will be there in  $32\text{ K} \times 4$  memory?

Answer ( [Please click here to Add Answer](#) )

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Generally two types of D/A Converters are used. Write down their names.

Answer ( [Please click here to Add Answer](#) )

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Draw the function table of an Half adder circuit.

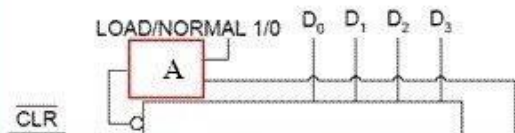
Answer ( [Please click here to Add Answer](#) )

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Following is an incomplete diagram. Name the gate which can be placed in red boxes A and B to configure 74HC161 as a Mod-9 counter.



Answer ( [Please click here to Add Answer](#) )

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Draw a circuit diagram of flip-flop based static memory cell.

Answer ( [Please click here to Add Answer](#) )

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What is RAM Stack, which register stores the address of top of the stack?

Answer ( [Please click here to Add Answer](#) )

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Simplify the following Boolean expression so that it uses minimum number of gates.

$$\overline{(A+B+C+D)} + \overline{(ABC)}$$

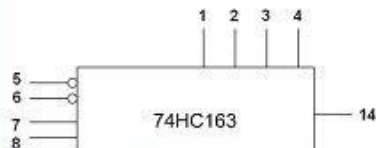
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You are given the block diagram of 74HC163 4-bit Synchronous Counter. Connect two 74HC163 4-bit Synchronous Counters to form a single Cascaded Decade Counter.



Answer ( [Please click here to Add Answer](#) )

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State table for a mealy machine is given below. Derive a state diagram for mealy machine from this state table.

Present State	Next State				Output Z			
	XY 00	XY 01	XY 10	XY 11	XY 00	XY 01	XY 10	XY 11
A	A	C	B	C	0	1	0	1
B	B	D	C	D	0	0	0	0

Answer ( [Please click here to Add Answer](#) )

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What is operational amplifier and how it can be used as an inverting amplifier? Write down the relation for its voltage gain.

Answer ( [Please click here to Add Answer](#) )

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What is the basic function of a comparator?

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Answer ( Please [click here](#) to Add Answer )



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What is meant by state assignment process?

Answer ( Please [click here](#) to Add Answer )

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**Made by: Waqar Siddhu**

On the fifth clock pulse, a 4-bit Johnson sequence is  $Q_0 = 0$ ,  $Q_1 = 1$ ,  $Q_2 = 1$ , and  $Q_3 = 1$ . What will be the sequence after sixth clock pulse?  
(Assume  $Q_3$  represents the least significant bit)

Answer ( Please [click here](#) to Add Answer )

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What is meant by Monotonicity of Digital-to-Analog converters?

Answer ( Please [click here](#) to Add Answer )

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Convert each of the following decimal numbers to Excess-3 codes:

a) 13                      b) 43

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Answer ( Please [click here](#) to Add Answer )



13=01000110

43=01110110

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How can we calculate the frequency of an unknown signal?

Answer ( Please [click here](#) to Add Answer )

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The frequency of the unknown signal can be calculated by counting the number of clock pulses of the unknown signal and dividing the count number by the time interval in which the clock pulses are counted,

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Write down three characteristics of serial in / serial out 4-bit left shift register.

Answer ( Please [click here](#) to Add Answer )

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How DRAMs are different from SRAMs? Write three point of differences.

Answer ( [Please click here to Add Answer](#) )

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1. SRAM is static while DRAM is dynamic
2. SRAM is faster compared to DRAM
3. SRAM consumes less power than DRAM
4. SRAM uses more transistors per bit of memory compared to DRAM
5. SRAM is more expensive than DRAM
6. Cheaper DRAM is used in main memory while SRAM

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Draw the function table of Full adder circuit.

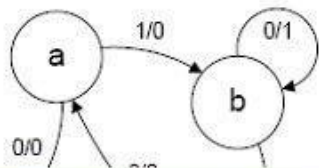
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Consider a state sequence **a, f, d, c, a, b, c, f, d, c**. Starting from initial state "a", draw a table for the inputs and outputs for the state diagram given below.



Answer ( [Please click here to Add Answer](#) )

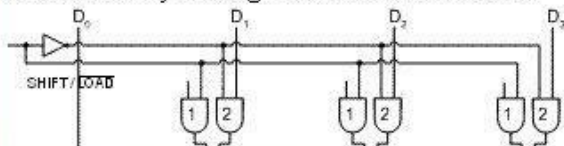
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Given below is an incomplete circuit diagram of parallel in / serial out shift register, in which  $Q_0$ ,  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and Clock input are disconnected. Connect above mentioned connections in such a way that functionality of the given circuit is not affected.



Answer ( Please [click here](#) to Add Answer )

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Memory chips can be connected together in different manners to increase the total size of the memory. Draw block diagram of 4K x word memory if you are given four 4K x bytes chips.

Answer ( Please [click here](#) to Add Answer )

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