Question No : 1 of 52   Marks: 1 (Budgeted Time 1 Min)

Caveman number system is Base _____ number system

Answer (Please select your correct option)

○ 2

○ 5   *correct*

○ 10

○ 16

Question No : 2 of 52   Marks: 1 (Budgeted Time 1 Min)

110 / 10 = _____

Note: both values are in binary

Answer (Please select your correct option)

○ 11   *correct*

○ 10

○ 111

○ 101

Question No : 3 of 52   Marks: 1 (Budgeted Time 1 Min)

The circuit diagram below explains the _____

Answer (Please select your correct option)

○ Associative Law for Multiplication

○ Commutative Law for Addition

○ Commutative Law for Multiplication

○ Associative Law for Addition   *correct*

$A + \overline{A}\,B =$ _____

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Answer (Please select your correct option)

○ A

○ B

○ A.B

○ A+B   correct   *Made by: Waqar Siddhu*

$\overline{A}B + \overline{A}B\overline{C} + AC$ is an example of _____

VuAnswers.com

Answer (Please select your correct option)

○ Product of sum form

○ Sum of product form   correct

○ Demorgans law

○ Associative law   *Made by: Waqar Siddhu*

A standard POS form has _____ terms that have all the variables in the domain of the expression.

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Answer (Please select your correct option)

○ Sum   correct

○ Product

○ Min

○ Composite   *Made by: Waqar Siddhu*

Question No : 7 of 52   Marks: 1 (Budgeted Time **1 Min**)

74HC163 has two enable input pins which are _____ and _____

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Answer (Please select your correct option)

- ○ ENP, ENT   correct
- ○ ENI, ENC
- ○ ENP, ENC
- ○ ENT, ENI

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Question No : 8 of 52   Marks: 1 (Budgeted Time **1 Min**)

Given the state diagram of an up/down counter, we can find _____

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Answer (Please select your correct option)

- ○ The next state of a given present state   correct
- ○ The previous state of a given present state
- ○ Both the next and previous states of a given state
- ○ The state diagram shows only the inputs/outputs of a given states

Made by: Waqar Siddhu

Question No : 9 of 52   Marks: 1 (Budgeted Time **1 Min**)

A multiplexer with a register circuit converts _____

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Answer (Please select your correct option)

- ○ Serial data to parallel
- ○ Parallel data to serial   correct
- ○ Serial data to serial
- ○ Parallel data to parallel

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Question No : 10 of 52   Marks: 1 (Budgeted Time 1 Min)

What will be output state when J = 1, K = 0 and CLR input is active?

Answer (Please select your correct option)

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○ Q = 1   *correct*

○ Q = 0

○ Retains previous output state

○ Toggle output   Made by: Waqar Siddhu

Question No : 11 of 52   Marks: 1 (Budgeted Time 1 Min)

When PRE' = 0 and CLR' =1, Qt = 0 then Q(t+1) will be _____

VuAnswers.com

Answer (Please select your correct option)

○ Output of flip-flop will be set (Logic 1)   *correct*

○ Output of flip-flop will be reset (Logic 0)

○ Output of flip-flop will be invalid

○ Flip-flop will change output on Clock transition   Made by: Waqar Siddhu

Question No : 12 of 52   Marks: 1 (Budgeted Time 1 Min)

Compared to analog systems, digital systems _____ .

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Answer (Please select your correct option)

○ are less prone to noise   *correct*   *not sure*

○ can represent an infinite number of values

○ can handle much higher power

○ occupy large space   Made by: Waqar Siddhu

Question No : 13 of 52
Marks: 1 (Budgeted Time 1 Min)

When one 1 is taken as a group on a Karnaugh map, the number of variables eliminated from the output expression is/are _____

Answer (Please select your correct option)

- 0
- 1
- 2 correct
- 3

Question No : 14 of 52
Marks: 1 (Budgeted Time 1 Min)

Determine the values of A, B, C, and D for the sum term $\bar{A} + B + \bar{C} + D$

Answer (Please select your correct option)

- $A = 1, B = 0, C = 0, D = 0$
- $A = 1, B = 0, C = 1, D = 0$ correct
- $A = 0, B = 1, C = 0, D = 1$
- $A = 1, B = 0, C = 1, D = 1$

Question No : 15 of 52
Marks: 1 (Budgeted Time 1 Min)

Determine the values of A, B, C, and D for the product term $\bar{A}B\bar{C}D$

Answer (Please select your correct option)

- $A = 0, B = 1, C = 0, D = 1$ correct
- $A = 1, B = 0, C = 1, D = 0$
- $A = 1, B = 1, C = 1, D = 1$
- $A = 0, B = 0, C = 1, D = 0$

Question No : 16 of 52   Marks: 1 (Budgeted Time 1 Min)

A transparent mode means _____

Answer (Please select your correct option)

○ Input Hold time is zero (no need to maintain input after clock transition)

○ The changes in the data at the inputs of the latch are seen at the output   *correct*

○ The changes in the data at the inputs of the latch are not seen at the output

○ Propagation Delay is zero (Output is immediately changed when clock signal is applied)

Question No : 17 of 52   Marks: 1 (Budgeted Time 1 Min)

The design and implementation of synchronous counters start from _____

Answer (Please select your correct option)

○ Truth table

○ K-map

○ State table

○ State diagram   *correct*

Question No : 18 of 52   Marks: 1 (Budgeted Time 1 Min)

The Sequential circuit whose output depends on the current state and the input is known as _____.

Answer (Please select your correct option)

○ Moore Machine

○ Mealy Machine   *correct*

○ Counter

○ Flip Flop

Question No : 19 of 52 Marks: 1 (Budgeted Time 1 Min)

The best state assignment tends to _____.

Answer (Please select your correct option)

○ Maximizes the number of state variables that don't change in a group of related states

correct

○ Minimizes the number of state variables that don't change in a group of related states

○ Minimizes the equivalent states

○ Maximizes the equivalent states

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Question No : 20 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____, the Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

Answer (Please select your correct option)

○ Moore machine

○ Mealy machine

○ Johnson counter

correct

○ Ring counter

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Question No : 21 of 52 Marks: 1 (Budgeted Time 1 Min)

Invalid state of NOR based SR latch occurs when _____

Answer (Please select your correct option)

○ S=0, R=0

○ S=0, R=1

○ S=1, R=0

○ S =1, R =1

correct   *Made by: Waqar Siddhu*

Question No : 22 of 52 Marks: 1 (Budgeted Time **1 Min**)

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

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Answer (Please select your correct option)

○ Doesn't have an invalid state

correct

○ Sets to clear when both J = 0 and K = 0

○ It does not show transition on change in pulse

○ It does not accept asynchronous inputs

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Question No : 23 of 52 Marks: 1 (Budgeted Time **1 Min**)

Following is the circuit diagram of mono-stable device. Which gate will be replaced by the red colored rectangle in the circuit?

+V

C   R

VuAnswers.com

Answer (Please select your correct option)

○ AND

○ XNOR

correct

○ NAND

○ NOR

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Question No : 24 of 52 Marks: 1 (Budgeted Time **1 Min**)

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is_____

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Answer (Please select your correct option)

○ 10 mW

○ 25 mW

correct

○ 64 mW

○ 84 mW

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Question No : 25 of 52   Marks: 1 (Budgeted Time 1 Min)

RCO Stands for _____

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Answer (Please select your correct option)

○ Reconfiguration Counter Output

○ Reconfiguration Clock Output

○ Ripple Counter Output

○ Ripple Clock Output   correct   *Made by: Waqar Siddhu*

Question No : 26 of 52   Marks: 1 (Budgeted Time 1 Min)

The Sequential circuit, whose output is determined by the current state only is known as _____.

VuAnswers.com

Answer (Please select your correct option)

○ Moore Machine   correct

○ Mealy Machine

○ Counter

○ Flip Flop   *Made by: Waqar Siddhu*

Question No : 27 of 52   Marks: 1 (Budgeted Time 1 Min)

In asynchronous transmission when the transmission line is idle, _____

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Answer (Please select your correct option)

○ It is set to logic low

○ It is set to logic high   correct

○ Remains in previous state

○ State of transmission line is not used to start transmission   *Made by: Waqar Siddhu*

Question No : 28 of 52 Marks: 1 (Budgeted Time 1 Min)

The output of this circuit is always _____.
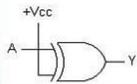
+Vcc

A ⊐⊐⊐— Y

Answer (Please select your correct option)

○ 1

○ 0

○ A   correct

○ A̅

Question No : 29 of 52 Marks: 1 (Budgeted Time 1 Min)

D — Q
CLK —▷ — Q̅
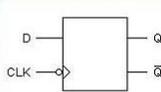
Which of the following statement is true regarding above block diagram ?

Answer (Please select your correct option)

○ Triggering takes place on the negative-going edge of the CLK pulse

○ Triggering takes place on the positive-going edge of the CLK pulse   correct

○ Triggering can take place anytime during the LOW level of the CLK waveform

○ Triggering can take place anytime during the LOW level of the CLK waveform

Question No : 30 of 52 Marks: 1 (Budgeted Time 1 Min)

Which is not characteristic of a shift register?

Answer (Please select your correct option)

○ Serial in/parallel in   correct

○ Serial in/parallel out

○ Parallel in/serial out

○ Parallel in/parallel out

A bidirectional 4-bit shift register is storing the nibble 1110. Its RIGHT/LEFT input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

Answer (Please select your correct option)

○ 1110

○ 0111

○ 1000

○ 1001   *correct*

Smallest unit of binary data is a _____

Answer (Please select your correct option)

○ Bit   *correct*

○ Nibble

○ Byte

○ Word

The high density FLASH memory cell is implemented using _____

Answer (Please select your correct option)

○ 1 floating-gate MOS transistor   *correct*

○ 2 floating-gate MOS transistors

○ 4 floating-gate MOS transistors

○ 6 floating-gate MOS transistors

Question No : 34 of 52   Marks: 1 (Budgeted Time 1 Min)

FIFO is an acronym for _____

Answer (Please select your correct option)

○ First In, First Out   *correct*

○ Fly in, Fly Out

○ Fast in, Fast Out

○ None of given options

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Question No : 35 of 52   Marks: 1 (Budgeted Time 1 Min)

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Answer (Please select your correct option)

○ Read Only Memory

○ First In First Out Memory   *correct*

○ Flash Memory

○ Fast Page Access Mode Memory

Made by: Waqar Siddhu

Question No : 36 of 52   Marks: 1 (Budgeted Time 1 Min)

Stack is a _____

Answer (Please select your correct option)

○ Bust Flash Memory

○ FIFO memory

○ LIFO memory   *correct*

○ Flash Memory

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Question No : 37 of 52   Marks: 1 (Budgeted Time 1 Min)

The voltage gain of the Inverting Amplifier is given by the relation _____

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Answer (Please select your correct option)

○ $V_{out} / V_{in} = - R_f / R_i$ correct

○ $V_{out} / R_f = - V_{in} / R_i$

○ $R_f / V_{in} = - R_i / V_{out}$

○ $R_f / V_{in} = R_i / V_{out}$

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Question No : 38 of 52   Marks: 1 (Budgeted Time 1 Min)

The process of converting the analogue signal into a digital representation (code) is known as _____

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Answer (Please select your correct option)

○ Strobing

○ Amplification

○ Quantization   correct

○ Digitization

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Question No : 39 of 52   Marks: 1 (Budgeted Time 1 Min)

A hold action occurs :

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Answer (Please select your correct option)

○ After the analog-to-digital conversion

○ During each sample

○ Immediately after a sample   correct

○ Before each sample

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Question No : 40 of 52 Marks: 1 (Budgeted Time 1 Min)

According to the sampling theorem, the sampling frequency should be :

Answer (Please select your correct option)

○ Greater than the lowest signal frequency

○ Less than half the lowest signal frequency

○ Greater than twice the highest signal frequency   correct

○ Less than half the highest signal frequency

Question No : 41 of 52 Marks: 2 (Budgeted Time 4 Min)

What is the basic function of a comparator?

Answer (Please click here to Add Answer)

Question No : 42 of 52 Marks: 2 (Budgeted Time 4 Min)

What is meant by state assignment process?

Answer (Please click here to Add Answer)

Question No : 43 of 52   Marks: 2 (Budgeted Time 4 Min)

On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. What will be the sequence after sixth clock pulse?
(Assume Q3 represents the least significant bit)

Answer (Please **click here** to Add Answer)

Question No : 44 of 52   Marks: 2 (Budgeted Time 4 Min)

What is meant by Monotonicity of Digital-to-Analog converters?

Answer (Please **click here** to Add Answer)

Question No : 45 of 52   Marks: 3 (Budgeted Time 6 Min)

Convert each of the following decimal numbers to Excess-3 codes:
a) 13   b)43

Answer (Please **click here** to Add Answer)

13=01000110

43=01110110

How can we calculate the frequency of an unknown signal?

Answer (Please click here to Add Answer)

The frequency of the unknown signal can be calculated by counting the number of clock pulses of the unknown signal and dividing the count number by the time interval in which the clock pulses are counted,

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Write down three characteristics of serial in / serial out 4-bit left shift register.

Answer (Please click here to Add Answer)

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How DRAMs are different from SRAMs? Write three point of differences.

Answer (Please click here to Add Answer)

1. SRAM is static while DRAM is dynamic
2. SRAM is faster compared to DRAM
3. SRAM consumes less power than DRAM
4. SRAM uses more transistors per bit of memory compared to DRAM
5. SRAM is more expensive than DRAM
6. Cheaper DRAM is used in main memory while SRAM

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Question No : 49 of 52   Marks: **5** (Budgeted Time **10 Min**)

Draw the function table of Full adder circuit.

Answer (Please **click here** to Add Answer)

Question No : 50 of 52   Marks: **5** (Budgeted Time **10 Min**)

Consider a state sequence **a, f, d, c, a, b, c, f, d, c**. Starting from initial state "a", draw a table for the inputs and outputs for the state diagram given below.

Answer (Please **click here** to Add Answer)

Question No : 51 of 52   **Marks: 5 (Budgeted Time 10 Min)**

Given below is an incomplete circuit diagram of parallel in / serial out shift register, in which Q0, Q1, Q2, Q3, and Clock input are disconnected. Connect above mentioned connections in such a way that functionality of the given circuit is not affected.
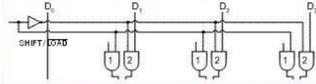
Answer (Please click here to Add Answer)

Question No : 52 of 52   **Marks: 5 (Budgeted Time 10 Min)**

Memory chips can be connected together in different manners to increase the total size of the memory. Draw block diagram of 4K x word memory if you are given four 4K x bytes chips.

Answer (Please click here to Add Answer)