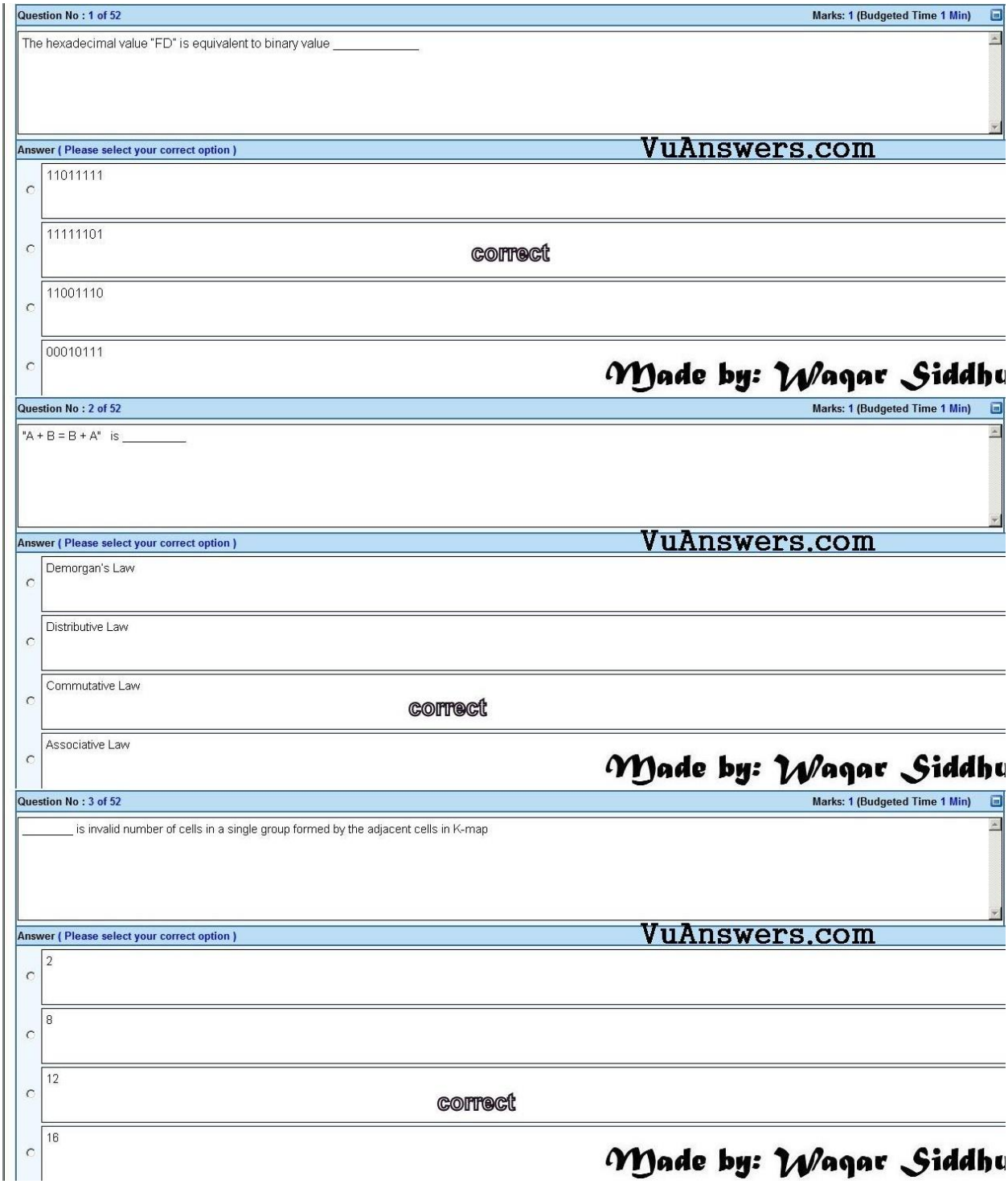
CS302 Final Term Papers By Waqar (File 4)



Question No : 1 of 52 Marks: 1 (Budgeted Time 1 Min)

The hexadecimal value "FD" is equivalent to binary value _____

Answer (Please select your correct option)

- 11011111
- 11111101 — correct
- 11001110
- 00010111

Question No : 2 of 52 Marks: 1 (Budgeted Time 1 Min)

"A + B = B + A" is _____

Answer (Please select your correct option)

- Demorgan's Law
- Distributive Law
- Commutative Law — correct
- Associative Law

Question No : 3 of 52 Marks: 1 (Budgeted Time 1 Min)

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

Answer (Please select your correct option)

- 2
- 8
- 12 — correct
- 16

Question No : 4 of 52 Marks: 1 (Budgeted Time 1 Min)

The _____ Encoder is used as a keypad encoder.

Answer (Please select your correct option)

- 2-to-8 encoder
- 4-to-16 encoder
- BCD-to-Decimal
- Decimal-to-BCD Priority

correct

Question No : 5 of 52 Marks: 1 (Budgeted Time 1 Min)

The Programmable Array Logic (PAL) has _____ AND array and a _____ OR array

Answer (Please select your correct option)

- Fixed, programmable
- Programmable, fixed

correct

- Fixed, fixed
- Programmable, programmable

Question No : 6 of 52 Marks: 1 (Budgeted Time 1 Min)

74HC163 has two enable input pins which are _____ and _____

Answer (Please select your correct option)

- ENP, ENT

correct

- ENI, ENC
- ENP, ENC
- ENT, ENI

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Question No : 7 of 52 Marks: 1 (Budgeted Time 1 Min)

Given the state diagram of an up/down counter, we can find _____

Answer (Please select your correct option)

- The next state of a given present state — correct
- The previous state of a given present state
- Both the next and previous states of a given state
- The state diagram shows only the inputs/outputs of a given states

Question No : 8 of 52 Marks: 1 (Budgeted Time 1 Min)

A 4-bit parallel in / serial out shift register contains the value "0100", _____ clock signal(s) will be required to shift the value completely out of the register (i.e. to set the register to 0).

Answer (Please select your correct option)

- 1
- 2 — correct
- 3
- 4

Question No : 9 of 52 Marks: 1 (Budgeted Time 1 Min)

In Single-Precision Floating Point format, "exponent" is represented by _____ bits.

Answer (Please select your correct option)

- 8-bits
- 16-bits
- 32-bits — correct
- 64-bits

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Question No : 10 of 52 Marks: 1 (Budgeted Time 1 Min)

A particular Full Adder has _____ inputs and _____ output(s).

Answer (Please select your correct option)

- 2, 3
- 2, 2
- 3, 2 correct
- 3, 3

Question No : 11 of 52 Marks: 1 (Budgeted Time 1 Min)

Programmable Array Logic (PAL) has _____ input(s) and _____ output(s).

Answer (Please select your correct option)

- Single, multiple
- Multiple, single
- Single, single
- Multiple, multiple correct

Question No : 12 of 52 Marks: 1 (Budgeted Time 1 Min)

At S = 0 and R = 1, an active-HIGH SR latch is in _____ condition.

Answer (Please select your correct option)

- SET
- RESET correct not sure
- Invalid
- No change

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Question No : 13 of 52 Marks: 1 (Budgeted Time 1 Min)

At J = 1, and K = 1, output of JK Flip-flop will be _____

Answer (Please select your correct option)

- Set
- Reset
- Toggle

correct

- Invalid

Question No : 14 of 52 Marks: 1 (Budgeted Time 1 Min)

The negative edge triggered flip-flop changes state on _____

Answer (Please select your correct option)

- Positive half cycle of clock
- Negative half of clock
- Low-to-high transition of clock
- High-low transition of clock

correct

Question No : 15 of 52 Marks: 1 (Budgeted Time 1 Min)

When four 1's are taken as a group on a Karnaugh map, the number of variables eliminated from the output expression is/are _____

Answer (Please select your correct option)

- 1
- 2
- 3
- 4

correct

Question No : 16 of 52 Marks: 1 (Budgeted Time 1 Min)

The _____ output of first 74HC163 counter is connected to _____ and _____ inputs of other 74HC163 counter to form a single cascaded counter

Answer (Please select your correct option)

- RCO, ENT, ENP — correct
- ENT, RCO, ENP
- ENP, RCO, ENT
- RCO, ENI, ENC

Question No : 17 of 52 Marks: 1 (Budgeted Time 1 Min)

The design and implementation of synchronous counters start from _____

Answer (Please select your correct option)

- Truth table
- K-map
- State table
- State diagram — correct

Question No : 18 of 52 Marks: 1 (Budgeted Time 1 Min)

The best state assignment tends to _____.

Answer (Please select your correct option)

- Maximizes the number of state variables that don't change in a group of related states — correct
- Minimizes the number of state variables that don't change in a group of related states
- Minimizes the equivalent states
- Maximizes the equivalent states

Question No : 19 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____, the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

Answer (Please select your correct option)

- Moore machine
- Mealy machine
- Johnson counter
- Ring counter

correct

Question No : 20 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____, the Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

Answer (Please select your correct option)

- Moore machine
- Mealy machine
- Johnson counter

correct

- Ring counter

Question No : 21 of 52 Marks: 1 (Budgeted Time 1 Min)

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

Answer (Please select your correct option)

- 0
- 1

correct

- Invalid
- Input is invalid

Question No : 22 of 52 Marks: 1 (Budgeted Time 1 Min)

For a gated D-Latch, if EN=1 and D=1 then Q(t+1) = _____

Answer (Please select your correct option)

- 0
- 1
- Q(t)
- Invalid

Question No : 23 of 52 Marks: 1 (Budgeted Time 1 Min)

Which of the following is NOT a sequential circuit?

Answer (Please select your correct option)

- SR latch
- Counter

correct

- Full Adder
- JK Flip-flop

Question No : 24 of 52 Marks: 1 (Budgeted Time 1 Min)

Each stage of Master-slave flip-flop works in _____

Answer (Please select your correct option)

- One complete clock signal
- One fourth of the clock signal
- One third of the clock signal
- One half of the clock signal

correct

Question No : 25 of 52 Marks: 1 (Budgeted Time 1 Min)

The counter states can be determined by the formula: _____ ("n" represents the total number of flip-flops).

Answer (Please select your correct option)

- n^2 (n raise to power 2)
- n^2-1 (n raise to power 2 and then minus 1)
- 2^n (2 raise to power n) — correct
- 2^n-1 (2 raise to power n and then minus 1)

Question No : 26 of 52 Marks: 1 (Budgeted Time 1 Min)

RCO Stands for _____

Answer (Please select your correct option)

- Reconfiguration Counter Output
- Reconfiguration Clock Output
- Ripple Counter Output
- Ripple Clock Output — correct

Question No : 27 of 52 Marks: 1 (Budgeted Time 1 Min)

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

Answer (Please select your correct option)

- 10 Hz
- 50 Hz — correct
- 100 Hz
- 500 Hz

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Question No : 28 of 52 Marks: 1 (Budgeted Time 1 Min)

The alternate solution for a demultiplexer-register combination circuit is _____

Answer (Please select your correct option)

- Parallel in / Serial out shift register
- Serial in / Parallel out shift register — correct
- Parallel in / Parallel out shift register
- Serial in / Serial Out shift register

Question No : 29 of 52 Marks: 1 (Budgeted Time 1 Min)

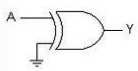
In asynchronous transmission when the transmission line is idle, _____

Answer (Please select your correct option)

- It is set to logic low
- It is set to logic high — correct
- Remains in previous state
- State of transmission line is not used to start transmission

Question No : 30 of 52 Marks: 1 (Budgeted Time 1 Min)

The output of this circuit is always _____.



Answer (Please select your correct option)

- 1
- 0
- A — correct
- $\overline{A}$

Question No : 31 of 52 Marks: 1 (Budgeted Time 1 Min)

Which is not characteristic of a shift register?

Answer (Please select your correct option)

- Serial in/parallel in
- Serial in/parallel out
- Parallel in/serial out
- Parallel in/parallel out

correct

Question No : 32 of 52 Marks: 1 (Budgeted Time 1 Min)

A Nibble consists of _____ bits

Answer (Please select your correct option)

- 2
- 4
- 8
- 16

correct

Question No : 33 of 52 Marks: 1 (Budgeted Time 1 Min)

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Answer (Please select your correct option)

- Write Time
- Refresh Time
- Refresh Time
- Access Time

correct

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Question No : 34 of 52 Marks: 1 (Budgeted Time 1 Min)

In _____, all the columns in the same row are either read or written.

Answer (Please select your correct option)

- Sequential Access
- MOS Access
- FAST Mode Page Access

correct

- None of given options

Question No : 35 of 52 Marks: 1 (Budgeted Time 1 Min)

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Answer (Please select your correct option)

- Read Only Memory
- First In First Out Memory

correct

- Flash Memory
- Fast Page Access Mode Memory

Question No : 36 of 52 Marks: 1 (Budgeted Time 1 Min)

The process of converting the analogue signal into a digital representation (code) is known as _____

Answer (Please select your correct option)

- Strobing
- Amplification
- Quantization

correct

- Digitization

Question No : 37 of 52 Marks: 1 (Budgeted Time 1 Min)

A hold action occurs :

Answer (Please select your correct option)

- After the analog-to-digital conversion
- During each sample
- Immediately after a sample
- Before each sample

Question No : 38 of 52 Marks: 1 (Budgeted Time 1 Min)

A flash A/D converter uses :

Answer (Please select your correct option)

- Counters
- Flip-flops
- Op-amps

correct

- An integrator

Question No : 39 of 52 Marks: 1 (Budgeted Time 1 Min)

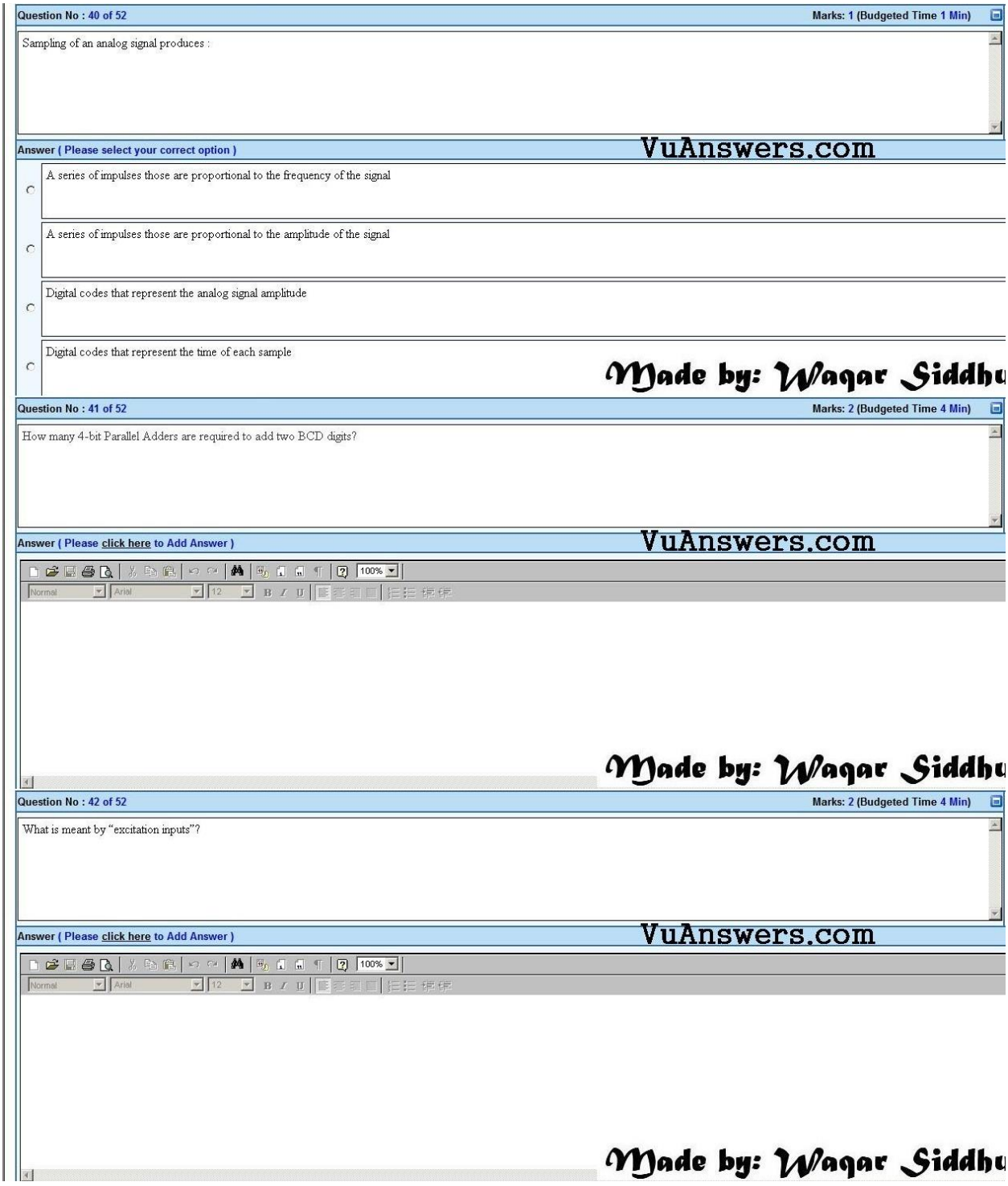
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

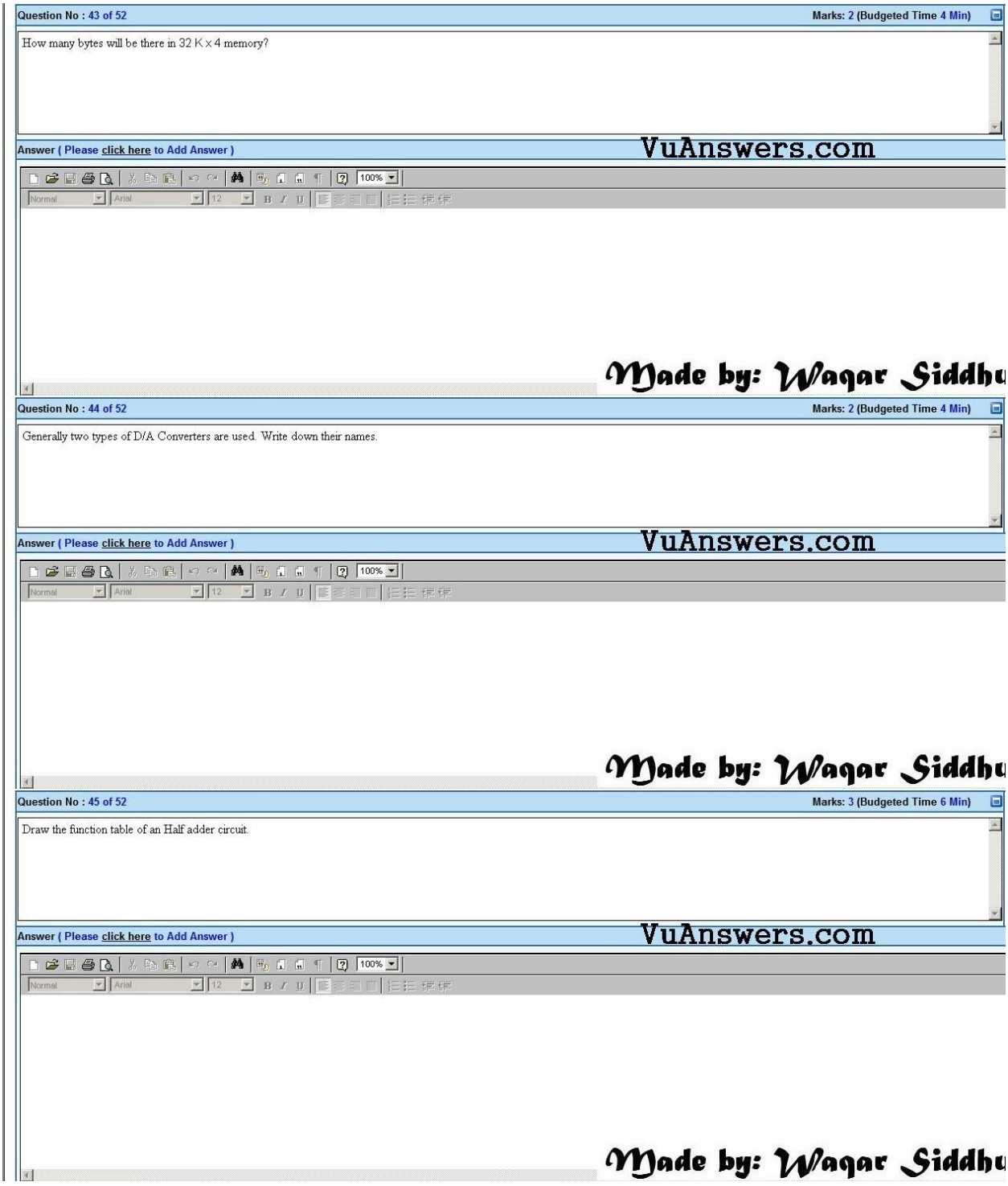
Answer (Please select your correct option)

- Resolution
- Accuracy

correct

- Quantization
- Missing Code





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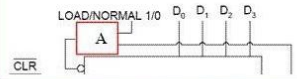
Question No : 46 of 52 Marks: 3 (Budgeted Time 6 Min)

Following is an incomplete diagram. Name the gate which can be placed in red boxes A and B to configure 74HC161 as a Mod-9 counter.



Answer (Please click here to Add Answer)

Question No : 47 of 52 Marks: 3 (Budgeted Time 6 Min)

Draw a circuit diagram of flip-flop based static memory cell.

Answer (Please click here to Add Answer)

Question No : 48 of 52 Marks: 3 (Budgeted Time 6 Min)

What is RAM Stack, which register stores the address of top of the stack?

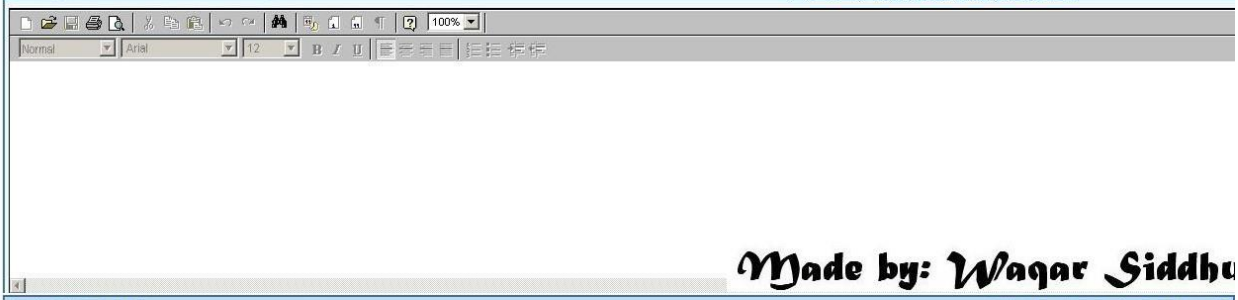
Answer (Please click here to Add Answer)

Question No : 49 of 52 Marks: 5 (Budgeted Time 10 Min)

Simplify the following Boolean expression so that it uses minimum number of gates.

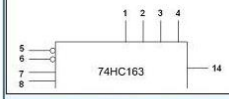
$\overline{(A+B+C+\overline{D})}+\overline{(ABC)}$

Answer (Please click here to Add Answer)

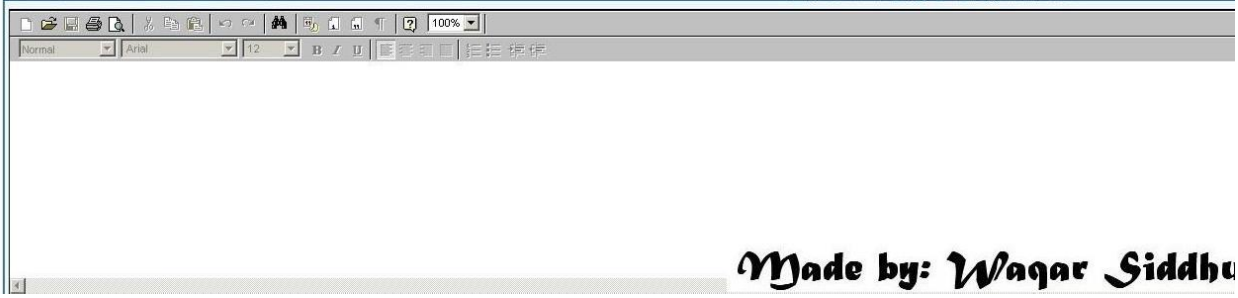


Question No : 50 of 52 Marks: 5 (Budgeted Time 10 Min)

You are given the block diagram of 74HC163 4-bit Synchronous Counter. Connect two 74HC163 4-bit Synchronous Counters to form a single Cascaded Decade Counter.



Answer (Please click here to Add Answer)



Question No : 51 of 52 Marks: 5 (Budgeted Time 10 Min)

State table for a mealy machine is given below. Derive a state diagram for mealy machine from this state table.

Present State	Next State				Output Z			
	XY 00	XY 01	XY 10	XY 11	XY 00	XY 01	XY 10	XY 11
A	A	C	B	C	0	1	0	1
B	B	D	C	D	0	0	0	0

Answer (Please click here to Add Answer)

Question No : 52 of 52 Marks: 5 (Budgeted Time 10 Min)

What is operational amplifier and how it can be used as an inverting amplifier? Write down the relation for its voltage gain.

Answer (Please click here to Add Answer)

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